BK5824 Datasheet

ETC OBU Transceiver

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1 General Description

The BK5824 is the high performance 5.8 GHz ETC transceiver for electronic toll collection compliant with GB/T 20851.1 -2007 and GB/T 20851.2-2007, which can be used at OBU with ASK modulation and demodulation.

The BK5824 is integrated with flexible wake-up circuit and three wake up mode. It has the legacy wake up mode to wake up by 14 kHz waveform. The second wake up mode will automatically wake up and check the 0x7E to determine either go to sleep or wake up MCU. The third mode is similar as the second mode, but it uses RSSI to wake up the system.

The BK5824 can receive the 1st BST without MCU control after wakeup, while keep ultra-low listen power.

The BK5824 needs very few external components. The low power design and high sensitivity make it very suitable for low-cost application and fast time to market.

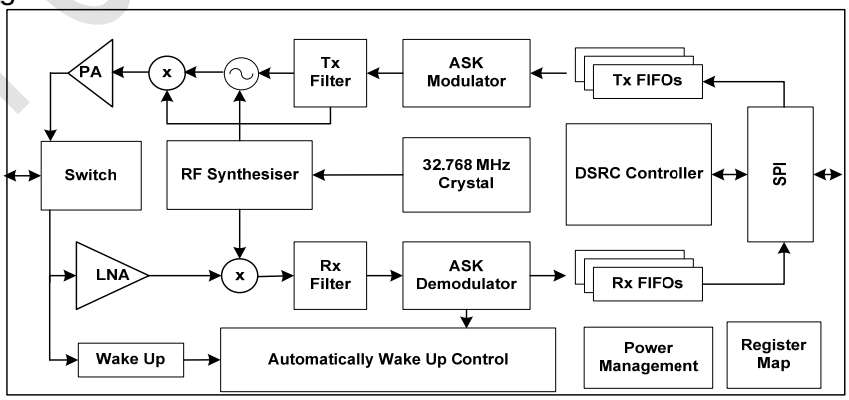
The BK5824 is available in QFN 28-Pin packages.

2 Features

- Frequency：5.7 GHz - 5.85 GHz
- Uplink 512 kbps/256 kbps
- Downlink 256 kbps/512 kbps
- Output power: Up to 7 dBm
- RX sensitivity: -85 dBm
- Wakeup sensitivity: -63dBm with external diode.
- -54dBm wakeup sensitivity without external diode and 4uA current consumption.
- 20 dB tuning range and 1dB tuning resolution for wake up sensitivity
- Wake up by 14 kHz waveform, 0x7E or RSSI
- Fast AGC to accommodate up to 85 dB dynamic range RF input
- Receiving the 1st BST without MCU control
- The sending CRC seed can auto adjust according to receiving CRC seed
- 2.6 V ~ 3.6 V supply
- 65 mA TX mode current
- 33 mA RX mode current
- 4-wires SPI up to 8 MHz

3 Application

- Electronic Toll Collection
- 5.8GHz Short Range Communication



4 Pin Information

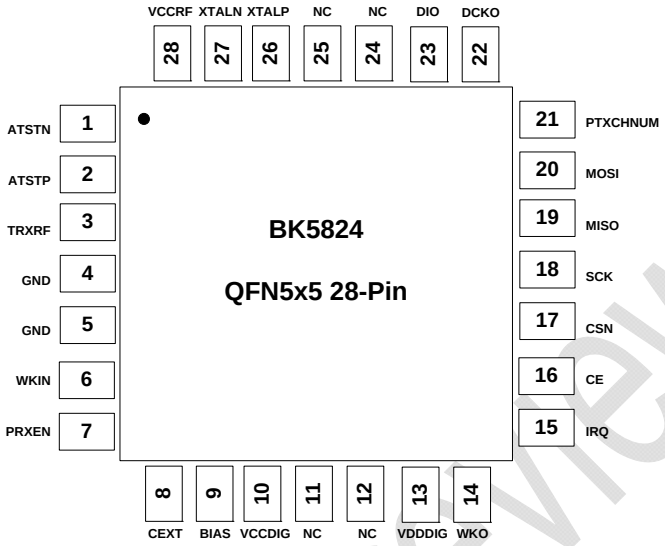


Figure 2 Package diagram

No.	Sym.	I/O	Function	Description
1	ATSTN			Analog test pin
2	ATSTP			Analog test pin
3	TRXRF			TRX RF input/output
4	GND	O	GND	Ground
5	GND	I	GND	Ground
6	WKIN			Wakup RF/IF input
7	PRXEN	I	Digital	Enable RX mode from pin (for pin model, if the RX control model is register model, this pin should be floating or vdd)
8	CEXT	I	Analog	De-coupling cap 15nF to VCC
9	BIAS	O	Analog	De-coupling cap 1nF to ground
10	VCCDIG	I	Power	2.6V~3.6V power supply input
11	NC	O		Reserved
12	NC		NC	
13	VDDDIG	O	Analog	De-coupling cap 1uF to ground
14	WKO	O	Analog	Wake-up signal detector output, which will generate a rising edge after the setting cycles of 14 kHz square wave.
15	IRQ	O	Interrupt	Interrupt for packet TX and RX
16	CE	I	Digital	Chip enable, active high
17	CSN	I	Digital	SPI enable input, active low
18	SCK	I	Digital	SPI clock input
19	MISO	O	Digital	SPI data output
20	MOSI	I	Digital	SPI data input

21	PTXCHNUM	I	Digital	Select TX channel number from pin(for pin control model, this pin should be floating or vdd for register model)
22	DCKO	O	Digital	Bit clock output
23	DIO	I/O	Digital	The TRX Data stream input/output
24	NC			Reserved
25	NC			Reserved
26	XTALP	I	Analog	32.768 MHz Crystal (+/-20ppm)
27	XTALN	O	Analog	32.768 MHz Crystal (+/-20ppm)
28	VCCRF	I	Power	2.6V~3.6V power supply input

5 Design Specification

5.1 Recommended Operating Conditions

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Supply Voltage	V_{CC}		2.6	—	3.6	V
Ambient Temperature	T_A		-40	25	85	°C

5.2 Absolute Maximum Ratings

Parameter	Symbol	Min	Typ	Max	Unit
Storage Temperature	T_{STG}	-55	—	150	°C
ESD (HBM) exclude RF pin		—	2	—	kV
ESD (HBM) RF pin			1.5		KV

5.3 AC Specification

Symbol	Parameter	Min.	Typ.	Max.	Unit
Operating Condition					
VDD	Voltage	2.6	3.3	3.6	V
TEMP	Temperature	-40	+27	+85	ºC
Digital Input Pin					
VIH	High level	0.7VDD	VDD	3.6	V
VIL	Low input		VSS	0.3VDD	V
Digital Output Pin					
VOH	High level (IOH=-0.25 mA)	VDD-0.3		VDD	V
VOL	Low level (IOL=0.25 mA)	VSS		0.3	V
RF/Analog					
FLO	Frequency	5770		5850	MHz
FXTAL	Crystal		32.768		MHz
Transmitter					
PRF	Output power		0	3	dBm
M	ASK modem depth	0		94	%
PRFC	Output power range		15		dB
PRFCR	Output power accuracy			±3	dB

PRF	30~1000 MHz			-36	dBm/100kHz
	2400~2483 MHz			-40	dBm/1MHz
	3400~3530 MHz			-40	dBm/1MHz
	5725 MHz~5850 MHz		-37	-33	dBm/100kHz
	Otherwise 1 GHz~20 GHz			-30	dBm/1MHz
IVDDMAX	TX Current (MAX. output power)		65		mA
TXDR	TX Data Rate		512		Kbps
OBW	Occupied Bandwidth		2.3	4.5	MHz
ACPR	Adjacent channel power rejection			-47	dB
Receiver					
RXMAX	Maximum input (10^{-5} BER)		0		dBm
RXSEN	Sensitivity (10^{-5} BER)		-85		dBm
IVDD	RX current		33		mA
TLO	LO settling time			40	us
FDR	RX data rate	253	256	259	Kbps
PCO	Co-channel selectivity		12		dBc
PAC	Adjacent selectivity		8		dBc
Block	Block interference		-30		dBc
Wake-up					
RXSEW1	Sensitivity with external diode		-63		dBm
RXSEW2	Sensitivity without external diode		-54		dBm
Isleep	Sleep current with no signal input		4		uA
TWK	Wake-up time		0.25		ms
Idle					
Iidle	Idle Current		4		mA
ShutDown					
Isd	Shut down current(CE=0)			0.1	uA
SPI					
FSCK	SPI clock frequency			8	MHz

6 Function Description

6.1 Receiver

6.1.1 Receiver Description

Figure3 is the block diagram of receiver. The receiver of BK5824 uses low-IF architecture and there is a 2-order 7.5MHz LPF behind mixer.

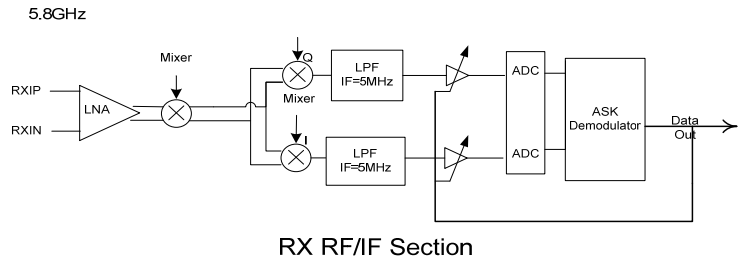


Figure 3 Receiver Block diagram

If set LO frequency to 5.835GHz, BK5824 will detect both 5.83 GHz and 5.84 GHz channel simultaneously, and automatically select the channel with high quality.
The RX LO should be set with setting below: Reg6 rxsdm<31:0>=0X76B6A000, Reg8<13:6> Ncal_rx<7:0>=0X77. if set LO frequency 5.825GHz, BK5824will only receive the 5.83GHz channel(set reg9<14> lpf_en=1), if set LO frequency 5.845GHz, BK5824will only receive the 5.84GHz channel(set reg9<14> lpf_en=1).

To enter RX mode, the MCU should write REGF rx_en=1. At RX mode, the BK5824 will automatically issue an interrupt and return to idle mode after receiving a packet. It will go back to RX mode after FIFO is read empty or interrupt flag is cleared. If BK5824 doesn't receive a whole packet, it will still be RX mode. If user want BK5824 enter idle mode, user should set rx_en in REGF to 0. BK5824 would enter into idle mode, if BK5824 doesn't received packet end 4ms behind the packet header arrives.

If user want BK5824 enter idle mode from sleep mode, CE pin and pwr_up in REG9 should be set to 1.

BK5824 can enter into RX model from sleep mode automatically too, if the Reg9<31> is set to "1", in this mode, BK5824 would enter into RX model automatically after the wakeup signal is detected. If set the Reg9<10>="1",. the BK5824 will return back the sleep mode, but you should set the Reg9<10>= "0" again in order to active the automatic wakeup mode again.

The BK5824 integrated a clock recover circuit. This circuit make BK5824 could endure ±1% data rate shift.

We regard as the manual RX mode as RX1, the automatic RX mode as RX2. In RX2 mode, BK5824 would return back sleep mode automatically if 7Eh hadn't been received in 1ms. BK5824 would go into idle mode if a packet is received, if the user want to return back RX2 mode, the RegF<1>rx_en should set "1", BK5824 would stay at RX2 mode until a packet is received.

6.1.2 Receiver AGC setting

To extend the dynamic range of BK5824's receiver, BK5824 integrated an AGC. There is two method AGC, one is fast mode, the other is slow mode, which is determined by Reg9<18:17> AGC_method. In fast mode, BK5824 would set the AGC very quickly in the short time; in slow mode, BK5824 will change the AGC slowly, you can set the

threshold value under this mode, if the received signal is smaller than the threshold value, BK5824 will regard this signal as the noise, so AGC would not change, the threshold is set through the REGA<24:11>, the suggested value of the threshold value is “200h”. in fast mode, the threshold isn’t useful.

Gain_rf_delay in REGB is used to set the delay time of AGC adjust. The suggested value is “1h”

6.1.3 Receiver CRC setting

Crc_enable in REGF is used to enable CRC checksum in TX and RX. If set 0 to crc_en, BK5824 will not do CRC check sum. Crc_seed is used to set the initial value of CRC. If set 1 to crc_rx_opt, BK5824 will do checksum by using 2 initial value “0” and “1” simultaneously.

6.1.4 RX RSSI

RSSI in REG3 indicates the received signal strength. User can get the RSSI information according to the value of RSSI and gain_rf in REG2, the unit of RSSI is dB. The table below indicates the relationship between the value of AGC gain_rf and actual RF gain. User can calculate the RSSI with following formula:

RSSI= x - y +56

X is the data of Reg3, y is the data of Reg2 corresponding value according the following table.

setting	gain(dB)
0x76	58
0x74	54
0x72	50
0x70	46
0x6a	42
0x68	38
0x62	34
0x60	30
0x42	26
0x40	22
0x2a	18
0x28	16
0x22	12
0x20	8
0x2	4
0x0	0

6.1.5 BER Test Mode

A continue time PN9 BER test is integrated in BK5824, Reg13 show the received bit number, Reg14 show the received error bit number, BER=reg13/reg14.

In RX1 mode, set Reg9<30>ber_en as “1”, Reg9<29> ber_hold=”0”, and toggle RegF<0>trx_rst(“1”->”0”->”1”) BK5824 begin to receive the PN9, the received bit number is show in Reg13, the error bit is show in Reg14. If Reg9<29>ber_hold=”1”, BK5824 stop the PN9 receiver process, the number in Reg13 and Reg14 would not change any more. If the user want to begin the above process again, the RegF<0>trx_rstn show be toggled before the above process.

6.2 Transmitter

6.2.1 Transmitter description

Figure 4 is the block diagram of BK5824’s transmitter. Ramp DAC controls the range of output carrier. To change output power and modulation depth, user can change the value of Ramp register. The ratio of maximum and minimum value of Ramp register decides modulation depth.

Tx power temperature compensation is integrated, the power will be controlled in the range 4dB from -40°C to 85°C.

The MCU should write the TX data to the FIFO, and pull CSN pin to high after one packet is filled. The BK5824 will begin transmission after detecting the rising edge of CSN and the delay time is passed ,which is set in reg9<8:7>TX_PLL_DELAY. and issue an interrupt and return to idle mode after FIFO is empty.

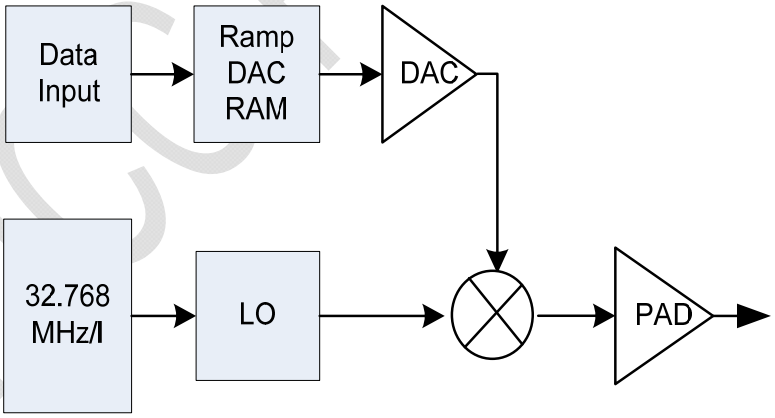


Figure 4 Transmitter Block Diagram

The transmit power can be set through REG9<4:1>rf_pwr control word, which can achieve 15 steps adjustment with up to 15 dB dynamic range.

The transmit carrier frequency is set with setting below.

5.8 GHz: Ncal_tx<7:0>=76h, txsdm<31:0>=0x76005555
5.79GHz: Ncal_tx<7:0>=76h, txsdm<31:0>=0x75CC4000
The BK5824 transmits the data in the FIFO with ASK modulation, whose modulation depth can be programmable with REG12.

$$A = \frac{ramp7\_kphigh - ramp0\_kplow}{ramp7\_kphigh + ramp0\_kplow}$$

The definition of ramp7_kphigh and ramp0_kplow is in the description of 9.4 ramping registers. By setting value of ramp7_kphigh and ramp0_kplow, the modulation depth of TX can be adjusted.
test_mode in RegF controls the transmit mode of transmitter. 2'b00 means normal data frame transmit mode. 2'b01 means random data transmit mode 2'b10 means all 0 data transmit mode. 2'b11 means transmit the data stream inputted from DO pin (need set data_oen in RegF to 1).

6.2.2 Transmitter CRC setting

If the regF<18> CRC_RX_OPT is set to "1", the sending CRC will be set automatically according to the received CRC value, otherwise the sending CRC would be set according to the regF<5> CRC_Seed.

If the regF<4> CRC_en is set "0" , no CRC will be added to the sending packet.

6.2.3 Transmitter Power setting

The transmitter power can be set through Reg9<4:1>rf_power.

6.2.4 Single Carrier setting

BK5824 enter into single carry transmitter mode through setting: reg2<7>txcwsel=1, reg9<0>pwr_up=1, regF<3:2>=01.

6.2.5 PN9 Modulation Signal setting

BK5824 enter into PN9 modulation mode through setting, reg2<7>txcwsel=0, reg9<0>pwr_up=1, regF<3:2>=01.

6.3 Wake-up Circuit

The wake-up circuit will output a high level at WKO pin after detecting setting cycles of 14 kHz square wave. The number of cycles is set by reg4<31:28>wkpn, the wake-up circuit can be reset by reg2<11>rstwk.

6.3.1 Wakeup mode

There exist two wakeup modes for BK5824, model 1 is automatic wakeup mode, model 2 is MCU Control model. For model 1, the BK5824 will enter into RX mode automatically if the wakeup signal is detected; for model 2 the BK5824 will output wko signal in pin wko if the wakup signal is detected, then MCU would detect the WKO output, then MCU is waked up, then MCU will control the BK5824 to receive the packet. the mode is set by reg9<31>

In mode 1, BK5824 will enter into RX mode automatically if the wakeup signal is detected, the user should set reg9<10>softwakeup_end to “1”, BK5824 will exit from the RX mode, then the user should set the reg9<10>softwakeup_end to “0” again, BK5824 will enter the automatic wakeup mode again.

In mode 1, two wakeup signal can be selected as the MCU wakeup signal, one is the 14KHz wakeup, the other is 7E, which is depended on the reg8<0>wk_sel. If wk_sel is “0”, Dwko pin will output “1” after 14KHz is detected , if wk_sel is “1” , Dwko pin will output “1” after 7Eh is detected.

In mode 2, when MCU detects high level on WKO, MCU can set registers through SPI in order to power up BK5824. After powered up, BK5824 will receive the data package transmitted by RSU.

6.3.2 Wakeup Band Pass Filter

In the baseband block of wake-up circuit, there is a BPF frequency discriminator. Only when the frequency of square wave is between Low limiter frequency and high limiter frequency , the square wave will be considered as wake-up wave. The low limiter and high limiter frequency can be set through the reg2<2:0>wlfsel and reg2<5:3>whfsel separately.

The frequency of BPF needs calibration. The calibration process is below:

1. Set 1 to roscdigcalsel in REG3<3>;
2. Set 1 to wu_cal in RegF<28> when BK5824 is under the idle mode;
3. After the 5ms, the calibration is done.

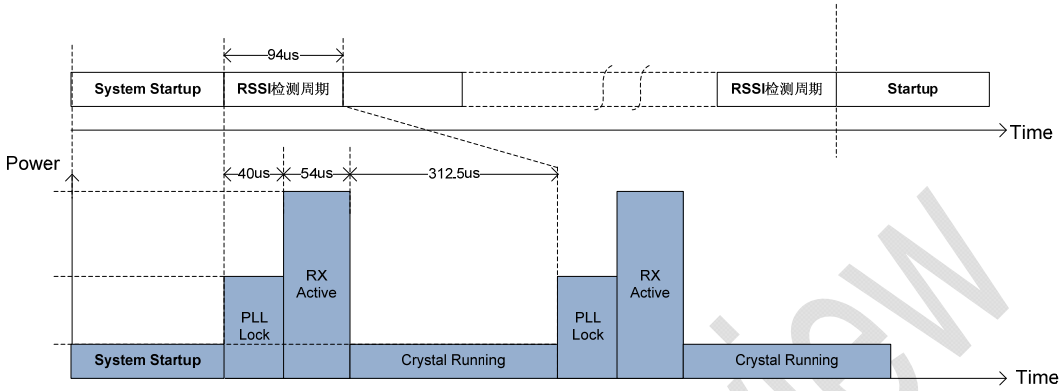
The frequency can be set manually If the Reg3<3>roscdigcalsel is set to “0” through the reg2<16:12>spirosc.

6.3.3 No Response Mode

The wakeup circuit would not response to the wakeup signal during the period of the setting time. In this mode, the current of BK5824 is about 6uA. The entrance into this mode is reg2<17>wkfibts, toggling this reg between “1” and “0”, BK5824 will enter this mode. The no response time can be set through reg2<8:6>wkstopt. The maximum time is 21.5s for 3’h111, the step is 3s, the minimum time is 0.5s.

6.3.4 Wakeup Timer mode

6.3.4.1 RSSI 唤醒时序

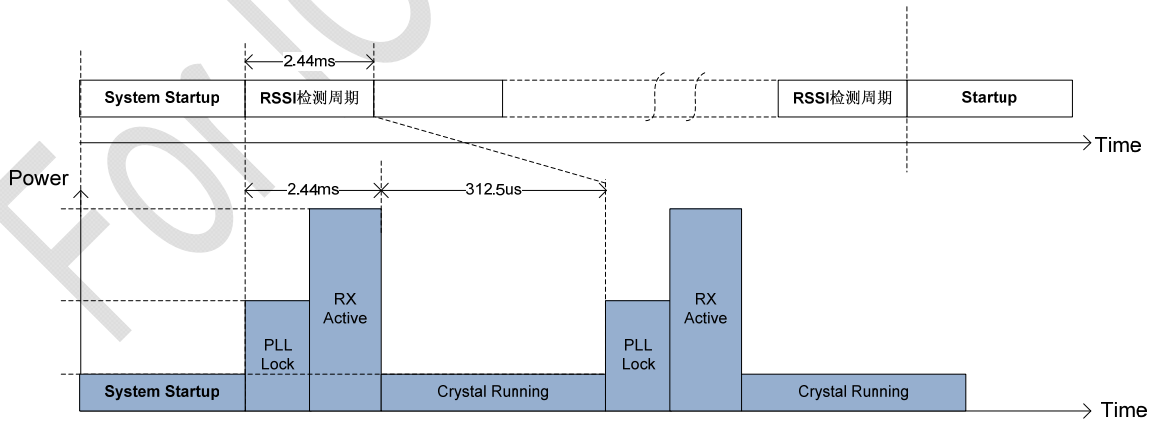


定期（RX_WAKEUP_INTERVAL[1:0]设置，0:0.5 秒，1:1 秒，2:2 秒，3:4 秒）执行一次上图的（典型值 10.1ms，实际由其他参数配置决定）检测模式，流程如下：

1. 系统从 Sleep 模式下进入 RX 模式等待晶体稳定
2. PLL 时钟锁定-时间设定为 40 us
3. 进行 RSSI 检测，时间可配置 RSSI_RX_DURATION[1:0]（0:54us，1:54us，2:85us，3:85us）
4. 保持晶体振荡-时间可配置 RSSI_IDLE_DURATION[2:0]（0:0.312ms；1:1ms；2:1.5ms；3:2ms）
5. rssi_wakeup_mode 设置为 1，irq_rssi_ena 设置为 1，检测 RSSI 的值并和门限比较 wakeup_db 比较，产生中断唤醒系统。

重复上述步骤 2,3,4 共 RSSI_DET_TIMES[1:0]（0: 5 次；1:9 次；2：13 次；3：25 次）。

6.3.4.2 0x7E 唤醒时序



定期（RX_WAKEUP_INTERVAL[1:0]设置，0:0.5 秒，1:1 秒，2:2 秒，3:4 秒）执行一次上图的（典型值 10.1ms，实际由其他参数配置决定）检测模式，流程如下：

1. 系统从 Sleep 模式下进入 RX 模式等待晶体稳定
2. PLL 时钟锁定-时间设定为 40 us
3. 进行 7E 检测，时间为 2.44ms。
4. 保持晶体振荡-时间可配置 RSSI_IDLE_DURATION[2:0]（0:0.312ms；1:1ms；2:1.5ms；3:2ms）

5. rssi_7e_mode 设置为 1，irq_7e_ena 设置为 1，检测到 7E 后，产生中断唤醒系统。
重复上述步骤 2,3,4 共 RSSI_DET_TIMES[1:0]（0: 5 次；1:9 次；2：13 次；3：25 次）。

6.4 State Machine

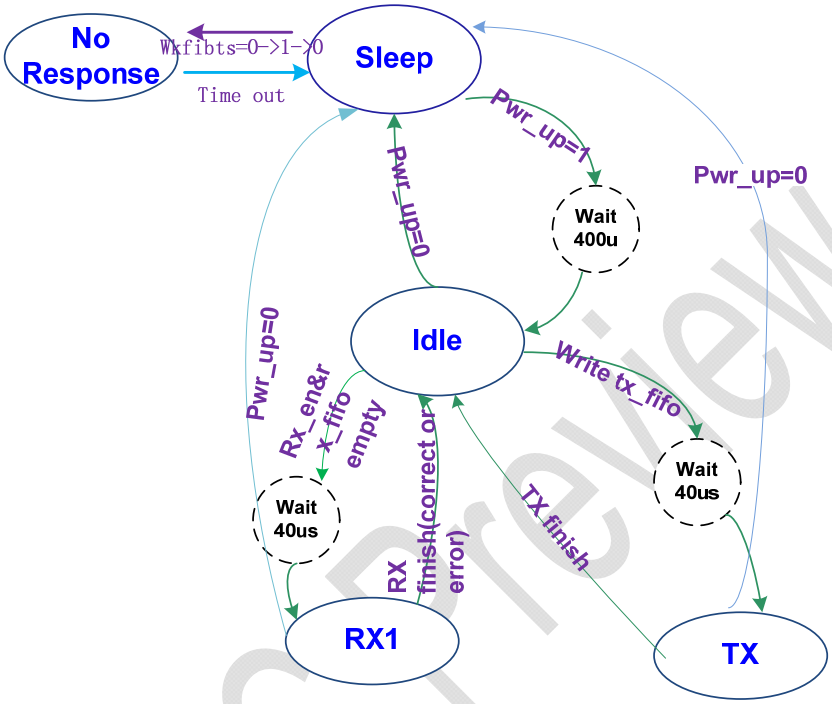


Figure 5 The BK5824 Manual wakeup Mode State Machine

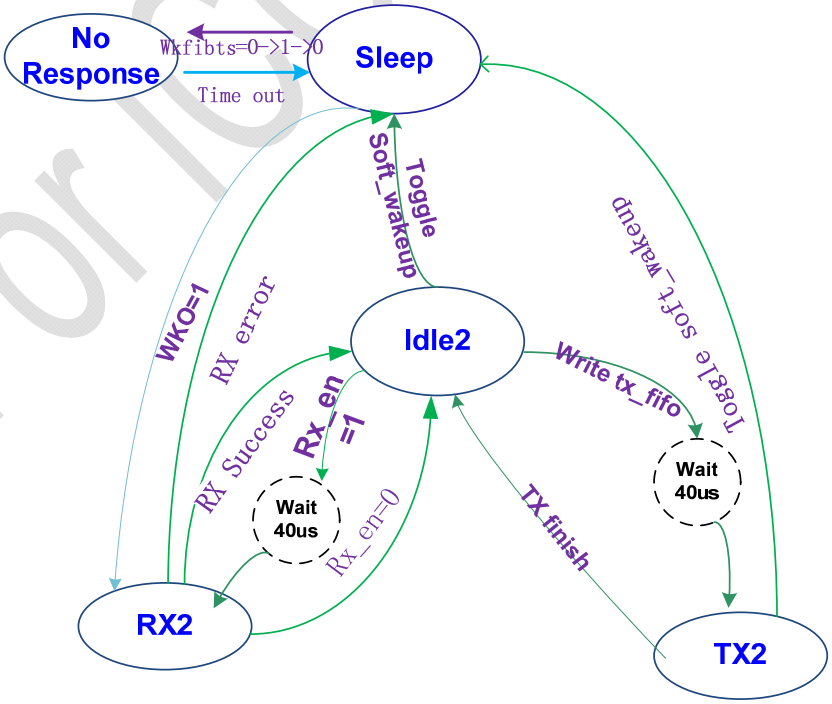


Figure 6 The BK5824 Automatic Wakeup Mode State Machine

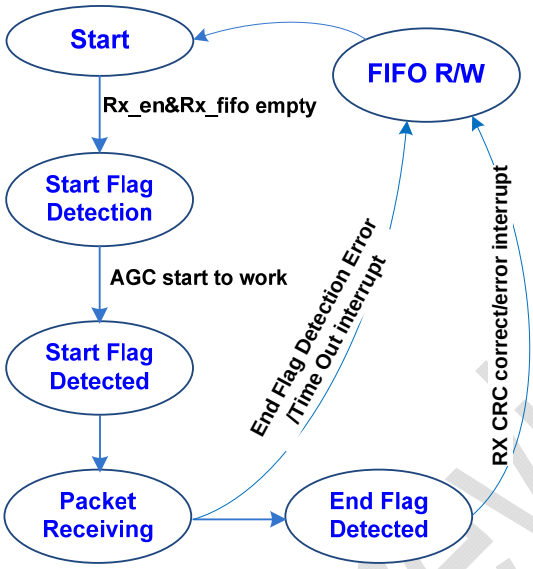


Figure 7 RX State Machine

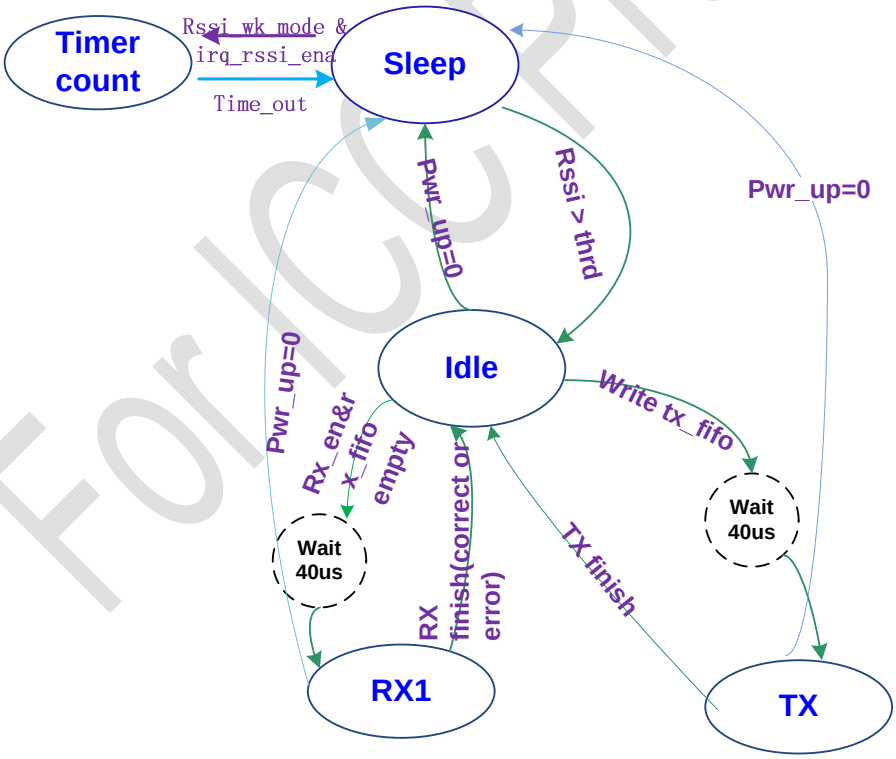


Figure 8 RSSI Wakeup Timer mode Machine

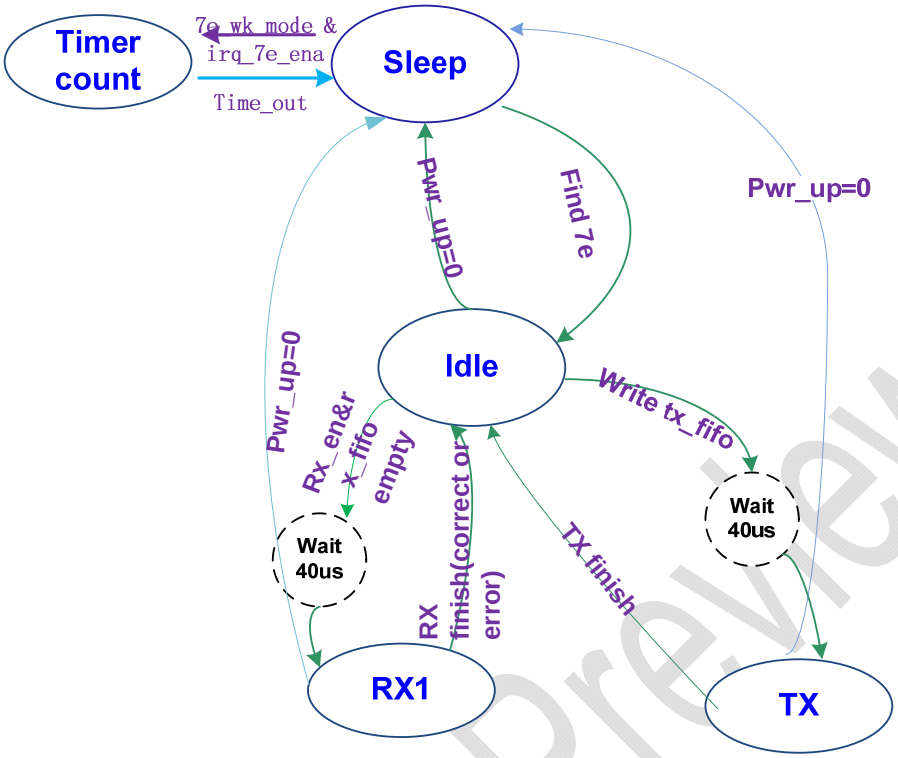


Figure 9 7E Wakeup Timer mode Machine

7 Control Interface

7.1 Basic Function

The control interface consists of one interrupt pin and a 4-pins SPI interface and the maximum frequency on SCK is 8MHz.

- IRQ: interrupt signal, low level valid
- CSN: SPI chip select signal
- SCK: SPI clock signal
- MOSI: Master Out Slave In, SPI data input signal
- MISO: Master In Slave Out, SPI data output signal

7.2 Operation and Timing

The SPI interface always transmits 8 bit command word firstly and then data bytes.

Abbr.	Description
Cn	SPI command word
Sn	State Register Bit Out
Dn	Data Bit (Note: Analog register is MSByte first, Digital and state control register is LSByte first. All bytes in every registers is MSBit first)

Operation	(c7-c0)	Description
Read	000AAAAA	AAAAA is the register address (MSB first)
Write	001AAAAA	AAAAA is the register address (MSB first)

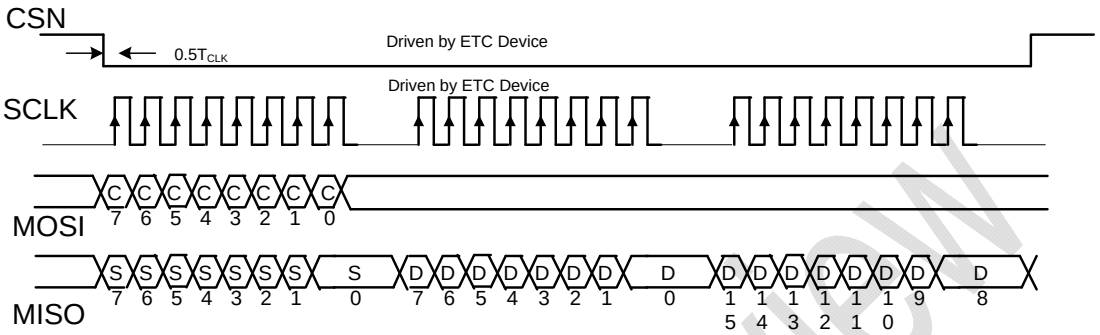


Figure 9 SPI Digital Register Read Timing

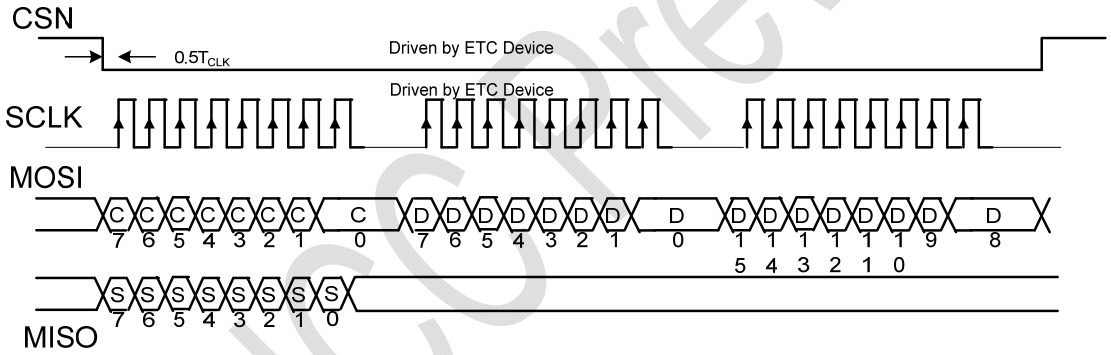


Figure10 SPI Digital Register Write Timing

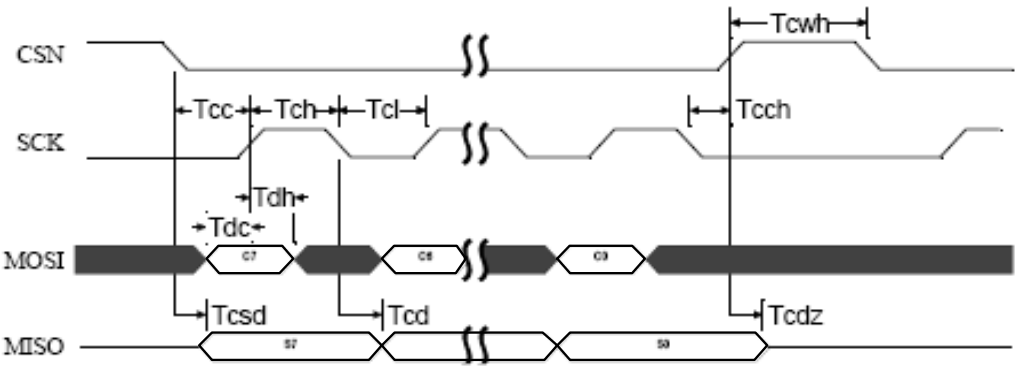


Figure 11 SPI Interface Timing

Symbol	Parameters	Min	Max	Units
Tdc	Data to **SCK** Setup	*2*		ns

Tdh	**SCK** to Data Hold	*2*		ns
Tcsd	**CSN** to Data Valid		*38*	ns
Tcd	**SCK** to Data Valid		*55*	ns
Tcl	**SCK** Low Time	*40*		ns
Tch	**SCK** High Time	*40*		ns
Fsck	**SCK** Frequency	*0*	*8*	MHz
Tr,Tf	**SCK** Rise and Fall		100	ns
Tcc	**CSN** to **SCK** Setup	*2*		ns
Tcch	**SCK** to **CSN** Hold	*2*		ns
Tcwh	**CSN** Inactive time	*50*		ns
Tcdz	**CSN** to Output High Z		*38*	ns

7.3 Data FIFO

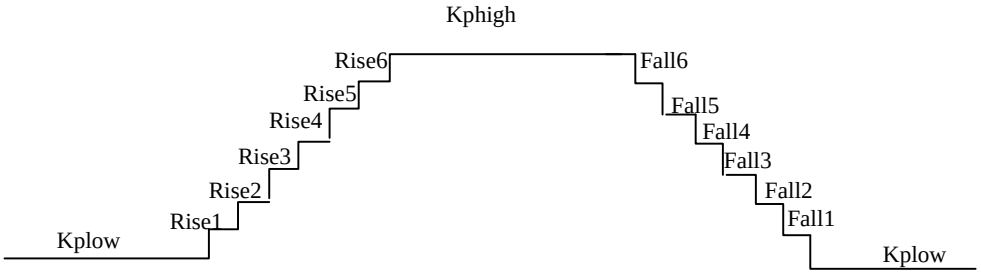
There is a 256-bytes FIFO in BK5824, which is used to store data packages to be sent or data packages received. Accessing data FIFO is accessing multi-bytes register virtually.

7.4 TX Ramping Control

The TX ramping curve is controlled by an 11 bytes ramping FIFO.

Addr. (12h)	Symbol	Definition	Suggested Value
87:84	Reserved		0
83:78	Ramp13_fall1	Ramping Down 1	38h
77:72	Ramp12_fall2	Ramping Down 1	38h
71:66	Ramp11_fall3	Ramping Down 1	38h
65:60	Ramp10_fall4	Ramping Down 1	0
59:54	Ramp9_fall5	Ramping Down 1	0
53:48	Ramp8_fall6	Ramping Down 1	0
47:42	Ramp7_Kphigh	Amplitude of “1”	0
41:36	Ramp6_rise6	Ramping up 6	0
35:30	Ramp5_rise5	Ramping up 5	0
29:24	Ramp4_rise4	Ramping up 4	0
23:18	Ramp3_rise3	Ramping up 3	38h
17:12	Ramp2_rise2	Ramping up 2	38h
11:6	Ramp1_rise1	Ramping up 1	38h
5:0	Ramp0_Kplow	Amplitude of “0”	38h

Register18 defines the envelope of TX as the figure below:



Modulation depth is defined by the expression below:

$$A = \frac{ramp7\_kphigh - ramp0\_kplow}{ramp7\_kphigh + ramp0\_kplow}$$

According to this expression, if set Kphigh as "0h", the value of Kplow can be calculated when we know the modulation depth.

8 Register Description

Address[bit]	Signal Name	Default Value	R/W	Function Statement
0x0[31]	lgdac	0x1	W	tx dac low gain control ,1: low gain, 0: high gain
0x0[30:29]	txfc<1:0>	0x3	W	tx baseband bandwidth selection. 3: highest bandwidth.
0x0[28:26]	txcgmsel<2:0>	0x4	W	tx constant gm bias resistor setting. 7: maximum current.
0x0[25]	divcgmsel	0x1	W	tx divider constant gm bias current selection.1:constant gm current, 0:atat current
0x0[24]	locgmsel	0x1	W	tx lo mixer constant gm bias current selection. 1: constant gm current.0: atat current.
0x0[23]	mixcgmsel	0x1	W	tx modulation mixer constant gm bias current selection. 1: constant gm current, 0: atat current.
0x0[22]	pacgmsel	0x1	W	Pa constant gm bias current selection. 1: constant gm current. 0: atat current.
0x0[21:20]	txloampc<1:0>	0x2	W	tx lo1 buffer tail resistor control. 3: no resistor, 2:600;1:1.2K; 0: 1.8K

0x0[19:18]	txdivampc<1:0>	0x2	W	tx divider current setting. 3: 1mA,2: 666uA, 1: 500uA, 0: 400uA
0x0[17:16]	txlo2ampc<1:0>	0x2	W	tx lo2 buffer tail resistor control. 3: no resistor, 2:1K , 1: 2K, 0: 0
0x0[15:12]	txlochsel<3:0>	0x8	W	tx lo load capacitor selection. 15:high frequency, 0: low frequency.
0x0[11:9]	txlongs<2:0>	0x4	W	tx lo mixer negative res setting, 7:high negative res setting.
0x0[8:7]	txloampc<1:0>	0x2	W	tx lo mixer current setting.00:2.4mA, 1:3mA, 2: 3.6mA, 3:4.2mA
0x0[6:3]	txmixchsel<3:0>	0x8	W	tx mixer(modulation) capacitor selection. 15:high frequency, 0: low frequency.
0x0[2:0]	NC<2:0>	0x4	W	
0x1[31:29]	paibs<2:0>	0x2	W	PA bias current setting. 7: maximum, 0: Minimum.
0x1[28:26]	pasvbc<2:0>	0x4	W	PA cascode nmos bias voltage selection. 7: vdd, 0: Minimum
0x1[25]	pavbsel	0x1	W	PA bias envelope follow voltage selection. 1: high voltage, 0: low voltage.
0x1[24:23]	paedts<1:0>	0x0	W	PA bias envelope follow res setting: 3: 15K, 2: 10K, 1: 5K, 0: 2.5K resistor selection
0x1[22]	enedts	0x0	W	enable PA bias envelope follow.1: enable. 0: disenable.
0x1[21]	ck32ken_k	0x0	W	32K rosc enable. 1: enable. 0: disenable.
0x1[20:18]	tstsel<2:0>	0x0	W	test pin source selection. 0~2: vdddig. 3: p=rosc_wk;n=wkcmpo; 4: RXIF vgao, 5:q_i2v, 6: I_i2v;7:vdacout
0x1[17:16]	ldovoc<1:0>	0x1	W	ldo output voltage selection. 3:2V, 2: 1.9V, 1:1.8V, 0:1.7V

0x1[15:14]	paldovoc<1:0>	0x1	W	PA ldo output voltage selection. 3:2V, 2: 1.9V, 1: 1.8V, 0:1.7V
0x1[13]	xosclpen	0x0	W	enable xtal osc low power mode. 1: enable.
0x1[12:10]	xamp[2:0]	0x4	W	xtal amplitude control. 7: high current.
0x1[9]	intcksel	0x1	W	intenal clock selection. 1: intenal clock.
0x1[8]	xqstarten	0x1	W	enable xtal quick start.1: enable.
0x1[7]	txcwsel	0x0	W	tx single carry wave enable. 1: enable.
0x1[6:0]	txmodin<6:0>	0x40	W	spi tx modulation input.
0x2[31:28]	lnacaps<3:0>	0x8	W	lna load cap selection. 15: Minimum cap. 0: maximum cap.
0x2[27:24]	lnapc<3:0>	0x7	W	lna current control. Thermometer code. 15: maximum current.
0x2[23:22]	NC	0x1	W	NC
0x2[21:18]	rxmix1caps<3:0>	0x8	W	rx mixer 1 load cap selection. 15: minimum cap. 0: maximum cap.
0x2[17]	wkstop	0x0	W	wakeup forbit function toggle.
0x2[16:12]	mrosc<4:0>	0x10	W	wakeup ring oscillator frequency manual setting.
0x2[11]	rstwk	0x0	W	reset wakup baseband.
0x2[10]	wktsten	0x0	W	enable wake up signal test output.
0x2[9]	acalen	0x0	W	wakeup rosc auto calibation enable. 1: enable.
0x2[8:6]	wkstopt<2:0>	0x0	W	wakeup forbit time setting. 0: 0.3s, 7:21s
0x2[5:3]	wkhfs<2:0>	0x4	W	wakeup frequency high side selection. 1K/step
0x2[2:0]	wklfs<2:0>	0x4	W	wakeup frequency low side selection. 0.5K/step
0x3[31:30]	msw<1:0>	0x0	W	manual rf switch setting. 00:state machine control. 01:wakeup path. 10: rx path. 11: tx path.
0x3[29]	mvco	0x0	W	manual vco enable. 1: vco enable. 0: state machine control.
0x3[28]	mpll	0x0	W	manual pll enable. 1: pll enable. 0: state machine control

0x3[27]	mtxlo	0x0	W	manual tx lo eanble. 1: txlo eanble. 0: state machine control.
0x3[26]	mtxmod	0x0	W	manual tx modulation enable. 1: tx modulation enable. 0: state machine control.
0x3[25]	mpa	0x0	W	manual tx pa enable. 1: pa enable. 0: state machine control.
0x3[24]	merrdet	0x0	W	manual pll unlock detection. 1: detection enable. 0: state machine control.
0x3[23]	mrxfe	0x0	W	manual rxfe enable. 1: rxfe enable. 0: state machine control.
0x3[22]	mrxlo	0x0	W	manual rx lo enable. 1: rxlo enable. 0: state machine control.
0x3[21]	mrxvga	0x0	W	manual rx vga enable. 1: rxvga enable. 0: state machine control.
0x3[20]	mrxadc	0x0	W	manual rx adc enable. 1: rxadc enable. 0: state machine control.
0x3[19]	mhgwk	0x0	W	manual high gain wakeup. 1: high gain wakeup enable. 0: state machine control.
0x3[18]	mlgwk	0x0	W	manual low gain wakeup 1: low gain wakeup enable. 0: state machine control.
0x3[17]	eniftst	0x0	W	enable if signal output for testing. 1:enable.
0x3[16]	ifhcc	0x0	W	enable if high current mode. 1: high current. 0: low current.
0x3[15]	g6dBi2v	0x0	W	i2v external 6dB gain enable. 1: enable. 0: disenable.
0x3[14:13]	rxmix2bs<1:0>	0x0	W	rx mixer 2 bias voltage selection.
0x3[12:10]	rxfebs<2:0>	0x4	W	rxfe constant gm resistor selection. 7: maximum current. 0: minimum current.
0x3[9:8]	rxlo2ampc<1:0>	0x1	W	rx lo2 buffer tail resistor control. 3: no resistor, 2:1K , 1: 2K, 0: 0
0x3[7:6]	rxdivampc<1:0>	0x1	W	tx divider current setting. 3: 1mA,2: 666uA, 1: 500uA, 0: 400uA
0x3[5:4]	txlo1ampc<1:0>	0x1	W	tx lo1 buffer tail resistor control. 3: no resistor, 2:600;1:1.2K; 0: 1.8K
0x3[3]	roscdigcalsel	0x1	W	wakeup rosc digital calibration enable. 1:enable.
0x3[2]	rxadcvrefc	0x0	W	rx adc vref selection.1: 0.6V, 0: 0.4V
0x3[1]	rxadcbias	0x0	W	rx adc bias current selection. 1: 2.5uA, 0: 5uA

0x3[0]	hgwken	0x0	W	enable rx wakup path. 1: enable(depend on the timer). 0: disenable.
0x4[31:28]	wkpn<3:0>	0x0	W	wakeup 14K squre wave number selection.
0x4[27:24]	wkcmpos<3:0>	0x8	W	wakup sensitivity setting. 0: minimum sensitivity. 1dB/step.
0x4[23:22]	wkhc<1:0>	0x0	W	wakeup high current mode. 3: maximum current.
0x4[21:19]	wkingset<2:0>	0x7	W	wakeup input gain setting. 7: maximum gain.
0x4[18:17]	wknwset<1:0>	0x0	W	wakeup loop nw setting. 0 : minmum voltage.
0x4[16]	wkibc2xen	0x0	W	wakeup 2x bias current selection. 1: enable.
0x4[15]	wkfagc	0x0	W	wakeup fast agc enable. 1:enable.
0x4[14:12]	wkhys_n<2:0>	0x0	W	wakup n hys setting. 0: no hys.
0x4[11]	wkcmosn_en	0x0	W	wakup cmpn os enable. 1: enable.
0x4[10]	wkcmosp_en	0x0	W	wakup cmpp os enable. 1: enable.
0x4[9:7]	wkhys_p<2:0>	0x0	W	wakup p hys setting. 0: no hys.
0x4[6:4]	wkicmpc<2:0>	0x0	W	wakup adc current control. 7: maximum current.
0x4[3:0]	wkibc<3:0>	0x0	W	wakup up global bias current setting. 0: minimum current.
0x5[31:0]	txsdm<31:0>	0x75cc4000	W	TX LO frequency 5790MHz

0x6[31:0]	rxsdm<31:0>	0x76b6a000	W	RX LO frequency 5835MHz
0x7[31]	sdmckpolsel	0x0	W	sdm_ck phase sel, 0 in phase
0x7[30]	int_mode	0x0	W	integer-N mode RFPLL
0x7[29]	manual	0x0	W	manually VCO freq .band operation (bypass AFC)
0x7[28]	spi_trigger	0x0	W	trigger AFC using 0-->1
0x7[27:22]	bandm<5:0>	0x0	W	manually VCO band input
0x7[21]	spi_reset	0x0	W	PLL reset signal
0x7[20]	TRSWen	0x1	W	trsw from ENCTRL module when=1, otherswise from spi
0x7[19]	TRSW_spi	0x0	W	0=tx mode, 1= rx mode
0x7[18]	capdirsel	0x0	W	no use
0x7[17]	errdet_spien	0x1	W	AFC trigger enable signal from Lock Detector unlock indictor
0x7[16:15]	hvref<1:0>	0x3	W	Lock Detector Comparator High Voltage Threshold
0x7[14:13]	lvref<1:0>	0x0	W	Lock Detector Comparator Low Voltage Threshold
0x7[12]	icp25uAen	0x1	W	PLL charge pump bias current adjust (0=10uA, 1=25uA)
0x7[11:10]	ckbiasvctrl<1:0>	0x2	W	VCO to DIV2 AC coupling biasing voltage adjust
0x7[9:7]	Nwvco<2:0>	0x4	W	Kvco linearity adjust
0x7[6:4]	Rvco<2:0>	0x4	W	VCO current biasing adjust
0x7[3]	Nrsten	0x1	W	Pscounter 8/9 reset enable signal
0x7[2]	refpolsel	0x0	W	PLL reference signal phase selection, 1 in phase
0x7[1]	tristate	0x0	W	PFD tristate control signal

0x7[0]	selvcopol	0x0	W	PFD input phase sel
0x8[31]	halfdelay_zero	0x0	W	PFD/CP dead-zone control signal
0x8[30]	ck16Men	0x1	W	PLL reference 32MHz enable
0x8[29:28]	ioffset<1:0>	0x0	W	Charge pump current offset adjust for linearity operation
0x8[27:26]	cp<1:0>	0x0	W	Charge pump charging/discharging current control
0x8[25:22]	loopresc<3:0>	0x4	W	PLL loop filter Resistor value control for Zero and phase margin
0x8[21:14]	Ncal_tx<7:0>	0x76	W	Divider N-value for Calibrating TX frequency using AFC
0x8[13:6]	Ncal_rx<7:0>	0x77	W	Divider N-value for Calibrating RX frequency using AFC
0x8[5]	wkispat	0x0	W	Reserved
0x8[4]	noConn	0x0	W	NC
0x8[3]	cal32k_trig	0x0	W	32K rosc trig
0x8[2]	noConn	0x0	W	NC
0x8[1]	Wkloadhg	0x0	W	Wakeup circuit high load setting
0x8[0]	wksel	0x0	W	Wakeup signal selection. “1h” for 7E “0h” for 14K
0x0[7:0]	chip_id	0x0	R	chip_id
0x1[7:0]	NC	0x0	R	NC
0x2[7]	hold	0x0	R	
0x2[6:0]	gain_rf	0x0	R	gain_rf
0x3[7:0]	rssi_db	0x0	R	rssi_db
0x4[6:0]	gain_rf_sync	0x0	R	gain_rf after sync
0x5[7:0]	Buf_cont<7:0>	0x0	R	Number of bytes in RX FIFO
0x6[7]	Rbuf_rdy	0x0	R	“0h”: RX FIFO is empty
0x6[6]	!Rbuf_rdy	0x0	R	
0x6[5]	Tbuf_rdy	0x0	R	“0h”: TX FIFO is empty
0x6[4]	!Tbuf_rdy	0x0	R	
0x6[3]	Osc_table	0x0	R	“1h” oscillator stable
0x6[2]	Rx_error_irt	0x0	R	RX error
0x6[1]	Rx_end_irt	0x0	R	RX packet end flag is received
0x6[0]	Tx_end_irt	0x0	R	TX packet is finished
0x7[4:0]	Wk_calvalue<4:0>	0x0	R	Wakeup calibration value If the awcalen is set to “1h”, this value will be work.
0x8[5]	irq_osc_sta	0x0	R	Osc_table
0x8[4]	irq_rssi_sta	0x0	R	rssi irq state
0x8[3]	irq_7e	0x0	R	irq_7e interrupt
0x8[2]	Rx_error_irt	0x0	R	RX error
0x8[1]	Rx_end_irt	0x0	R	RX packet end flag is received

0x8[0]	Tx_end_irt	0x0	R	TX packet is finished
0x9[31]	Wakeup_mode	0x0	W/R	Wake mode selection: “1h” auto mode “0h” manual mode
0x9[30]	Ber_en	0x0	W/R	RX bit error rate test enable “1h” enable “0h” disenable
0x9[29]	Ber_hold	0x0	W/R	RX bit error rate test hold “1h” hold
0x9[28]	Time_recov_opt	0x0	W/R	Clock Recovery Enable “0h”: disenable “1h”: enable
0x9[27]	Reserved	0x0	W/R	set to "1"
0x9[26]	sel_syncnew	0x0	W/R	同步方式选择 0：旧同步方式。 1：新同步方式。
0x9[25:22]	match_num	0x0	W/R	BK5824 同步的 match number，可以设置为 3
0x9[21]	sync_once	0x0	W/R	BK5824 同步方式选择。 0：一次接收可以同步多次。 1：一次接收只同步一次。
0x9[20]	clock_track_en	0x0	W/R	时钟 track 使能
0x9[19]	slice_track_en	0x0	W/R	slice track 使能
0x9[18:17]	AGC_Rate	0x0	W/R	AGC speed control “2’b00”: reserved “2’b01”: slow AGC “2’b10”: fast AGC “2’b11”: reserved Suggest to use fast AGC
0x9[16]	hd_opt	0x0	W/R	set to "0"
0x9[15]	env_det_opt	0x0	W/R	set to "0"
0x9[14]	lpf_en	0x0	W/R	Digital RX chain low pass filter enable “1h” enable “0h” disenable
0x9[13]	fm0_eq_en	0x0	W/R	fm0 equalizer 使能
0x9[12]	Dc_del	0x0	W/R	set to "1"
0x9[11]	rssi_sequ	0x0	W/R	set to "0"

0x9[10]	Soft_wakeupend	0x0	W/R	Return back the sleep mode from idle mode under auto wakeup mode. 1->0
0x9[9]	adc_lsb_10	0x0	W/R	set to "0"
0x9[8:7]	Tx_delay	0x0	W/R	TX delay “00” 40us “01” 60us “10” 80us “11” 100us
0x9[6:5]	Rx_delay	0x0	W/R	RX delay “00” 40us “01” 60us “10” 80us “11” 100us
0x9[4:1]	rf_pwr[4:1]	0x0	W/R	PA output power “0h”: Min. “1fh”: Max.
0x9[0]	Pwr_up	0x0	W/R	Mode “0h”: Sleep “1h”: Idle
0xa[24:11]	Hd_threshold	0x0	W/R	Noise threshold: If AGC_Rate is “2’b01”, set 200h; If AGC_Rate is “2’b10”, set 000h.
0xa[10:0]	Hd_points	0x0	W/R	set to "1FF"
0xb[31]	rf_pwr[0]	0x0	W/R	PA output power bit0
0xb[21]	frm_head_en	0x0	W/R	frm_head_rec 使能
0xb[20]	irq_rssi_ena	0x0	W/R	rssi irq enable
0xb[19]	irq_7e_ena	0x0	W/R	7e irq enable
0xb[18]	bit_out_sel	0x0	W/R	1:pre fm0_decoder 0:after fm0_decoder
0xb[17]	rx_pin_en	0x0	W/R	
0xb[16]	tx_num	0x0	W/R	
0xb[15]	bitclk_pwd	0x0	W/R	pwd bitclk output
0xb[14:8]	wakeup_db	0x0	W/R	rssi wakeup db

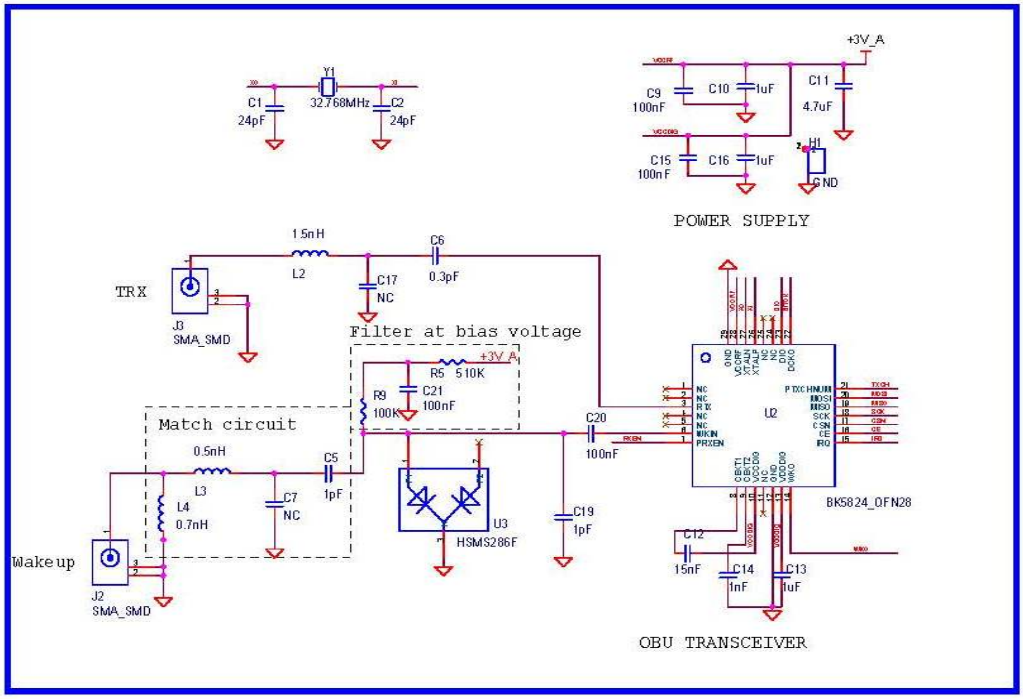
0xb[7:2]	Gain_rf_delay	0x0	W/R	AGC settling time control “0h”: Min. “3Fh”: Max “1h” is suggested
0xb[1:0]	Gain_rf_step	0x0	W/R	set to"0"
0xc[31:20]	Gt_points1	0x0	W/R	set to "400h" slow agc point setting.
0xc[19:10]	High_limiter1	0x0	W/R	“60h” slow agc threshold setting value
0xc[9:0]	Low_limiter1	0x0	W/R	“10h” slow agc threshold setting value
0xd[31:30]	rssi_wake_interval	0x0	W/R	定期唤醒设置，0:0.5 秒，1:1 秒，2:2 秒，3:4 秒
0xd[29:28]	rssi_rx_duration	0x0	W/R	0:40us，1:50us，2:60us，3:80us
0xd[27:26]	rssi_idle_duration	0x0	W/R	0:280us,1:1ms 2:1.5ms, 3:2ms
0xd[25:24]	rssi_det_time	0x0	W/R	0: 5 次；1:9 次；2：13 次；3：25 次
0xd[23]	rssi_wake_mode	0x0	W/R	Rssi wakeup enable
0xd[22]	ie7_wakeup_mode	0x0	W/R	7e wakeup enable
0xd[21]	sync_eq_en	0x0	W/R	BK5824 sync equalizer enable
0xd[20]	match_r_sel	0x0	W/R	使能 match_pattern 取反，即只要满足 match_pattern 或~match_pattern 其中之一都可以找到 sync
0xd[19:10]	high_limit2	0x0	W/R	“20h” fast agc threshold setting value
0xd[9:0]	low_limit2	0x0	W/R	“Fh” fast agc threshold setting value
0xe[31:0]	Match_pattern	0x0	W/R	
0xf[30]	irq_7e_clr	0x0	W/R	Clear 7e interrupt
0xf[29]	irq_rssi_clr	0x0	W/R	Clear rssi interrupt
0xf[28]	wu_cal	0x0	W/R	Wake-up calibration Software set, hardware clear

0xf[27]	irq_xtal_clr	0x0	W/R	Clear xtal start interrupt
0xf[26]	irq_rx_err_clr	0x0	W/R	Clear RX error interrupt
0xf[25]	irq_rx_clr	0x0	W/R	Clear RX interrupt
0xf[24]	irq_tx_clr	0x0	W/R	Clear TX interrupt
0xf[23]	irq_xtal_en	0x0	W/R	Enable xtal start interrupt
0xf[22]	irq_rx_err_en	0x0	W/R	Enable RX error interrupt
0xf[21]	irq_rx_en	0x0	W/R	Enable RX interrupt
0xf[20]	irq_tx_en	0x0	W/R	Enable TX interrupt
0xf[19]	Reserved	0x0	W/R	Reserved
0xf[18]	crc_rx_opt	0x0	W/R	“1”: use 0 and 1 to do CRC simultaneously “0”: only use the value of crc_seed to do CRC If “1” is set, the TX CRC will be set according to the received packet’s CRC.
0xf[17]	fm0_rx_err_opt	0x0	W/R	“1”: if received fm0 code is wrong, discard the data and receive again
0xf[16]	fm0_tx_opt	0x0	W/R	When transmit fm0, invert 0 and 1
0xf[15]	Data_oen	0x0	W/R	Pin22 DIO output enable “0h”: DIO output data “1h”: DIO input data
0xf[14]	Reserved	0x0	W/R	set to "0"

0xf[13]	Rxdatatrate	0x0	W/R	Rx date rate selection “1h” 512K “0h” 256K
0xf[12:11]	Txdata_rate	0x0	W/R	TX Data Rate “00”: 256K “01”: 125K “10”: 512K “11”: NA
0xf[10]	sqw14_en	0x0	W/R	TX 14KHz square wave “0h”: Disable “1h”: Enable
0xf[9:6]	Pack_pre	0x0	W/R	Number of symbol 1 between square wave and preamble
0xf[5]	crc_seed	0x0	W/R	CRC seed
0xf[4]	crc_enable	0x0	W/R	CRC enable “0h”: Disable “1h”: enable
0xf[3:2]	test_mode<1:0>	0x0	W/R	TX test mode “00”: Normal “01”: Random bit “10”: Transmit all 0 data
0xf[1]	rx_en	0x0	W/R	RX Enable “1h”: Enable “0h”: Disable
0xf[0]	Trx_rstn	0x0	W/R	Reset TX and RX “0h”: Reset “1h”: Work
0x10[7:0]	FIFO	0x0	W/R	TX and RX FIFO
0x11[111:0]	gain_rf_table	0x0	W/R	gain_rf_table
0x12[88:0]	tx_ramp_table	0x0	W/R	tx ramping table Defaultseeting: 0x0E38E00000000000E38E3

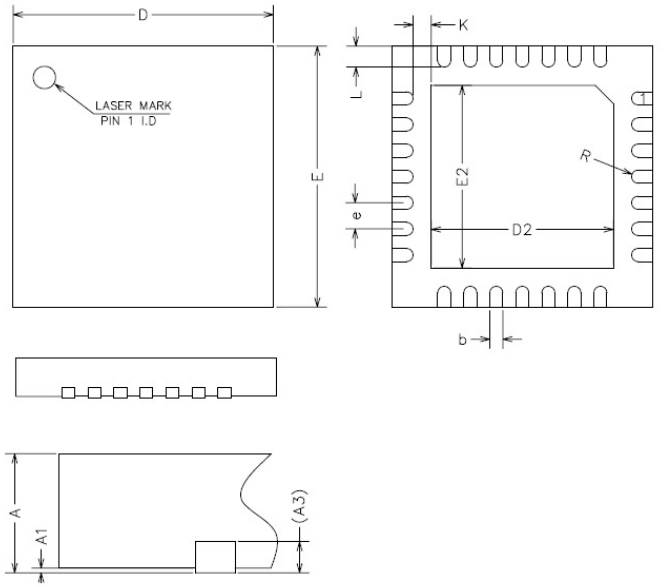
				8
0x13[31:0]	ber_num	0x0	W/R	The number of received bits under BER test mode
0x14[31:0]	ber_err	0x0	W/R	The number of error bits under BER test mode
0x18[31:0]	txsdmb<31:0>	0x76005555	W	TX LO frequency 5800MHz

9 Reference Circuit



10 Package information

BK5824 uses the QFN 5x5 28-pin packages.



COMMON DIMENSIONS
(UNITS OF MEASURE=MILLIMETER)

SYMBOL	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	0	0.02	0.05
A3		0.20REF	
b	0.20	0.25	0.30
D	4.90	5.00	5.10
E	4.90	5.00	5.10
D2	3.35	3.50	3.65
E2	3.35	3.50	3.65
e	0.40	0.50	0.60
K	0.20	–	–
L	0.30	0.40	0.50
R	0.09	–	–

11 Order information

Part number	Package	Packing	Minimum Order Quantity
BK5824QN	QFN 28-Pin	Tape Reel	3K

12 Update History

Version	Date	Author	Update Description
V0.1	2016-03-01	WF	Initial draft
V1.0	2016-12-30	Jz	Update