Wide Input Range Buck Converter

With Integrated Synchronous 2-Switchs

1. Features

- Wide Input Voltage Range from 4V to 32V
- Programmable V_{OUT} Range from 0.8V to 30V
- Peak Current Mode Control
- Integrated Two low Rdson N-MOSFETs
- Adjustable Cycle-by-Cycle Current Limit by ILIM
- Adjustable Frequency: 100kHz~1MHz
- External Soft-Start Limits the Input Inrush Current
- Selectable FCCM or DCM with Pulse Skipping
- Cable Impedance Compensation
- Low Dropout Operation with Maximum Duty Cycle at 99.5%
- Input Under-Voltage Lockout
- Output OCP, SCP, OVP
- Thermal Shutdown
- QFN-28 Package, 5mm×5mm×0.75mm

2. Applications

- USB Power Delivery Supply
- Car Charger
- USB Dedicated Charging Port
- Type-C Docks/Adapters
- Computer Peripherals

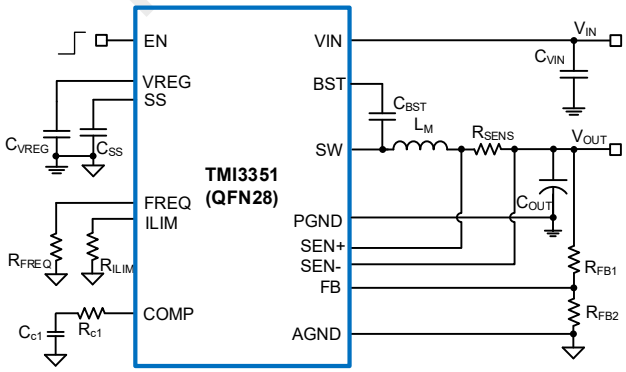
3. Description

The TMI3351 is an integrates 2-switchs synchronous buck converter mainly for widely varying input step-down regulator applications. The control method is based upon current mode control that enables maximum performance under transient conditions. The output voltage can be programmed by the FB pin. It operates as a Buck mode while the input voltage is sufficiently greater than the regulated output voltage and transitions to the low dropout operation mode with maximum duty cycle at 99.5% as the input voltage very approaches the output voltage.

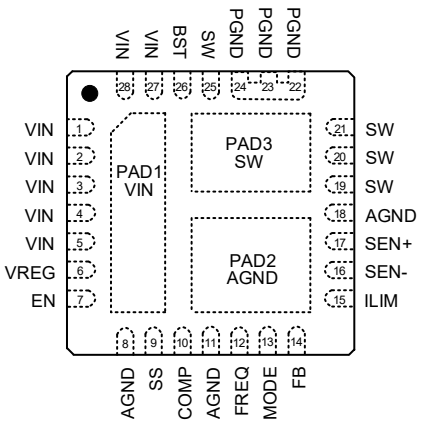
It also features an adjustable soft-start function and cable impedance compensation function and offers protection features including input UVLO, cycle-by-cycle current limit, over power protection (OPP), output short protection (SCP) or OVP and thermal shutdown. In addition, it features selectable Forced Continuous Conduction Mode (FCCM) or Discontinuous Conduction Mode (DCM) operation for light load condition.

The TMI3351 is available in compact QFN5x5-28.

4. Typical Application Circuit



5. Pin Configuration



6. Ordering Information

Part Number	Package	Top Marking[1]	Quantity / Reel
TMI3351	QFN-28 (5mm x 5mm)	T3351 XXXXX	3000

Note: 1. T3351: Device Code, 2. XXXXX: Inside Code

7. Block Diagram

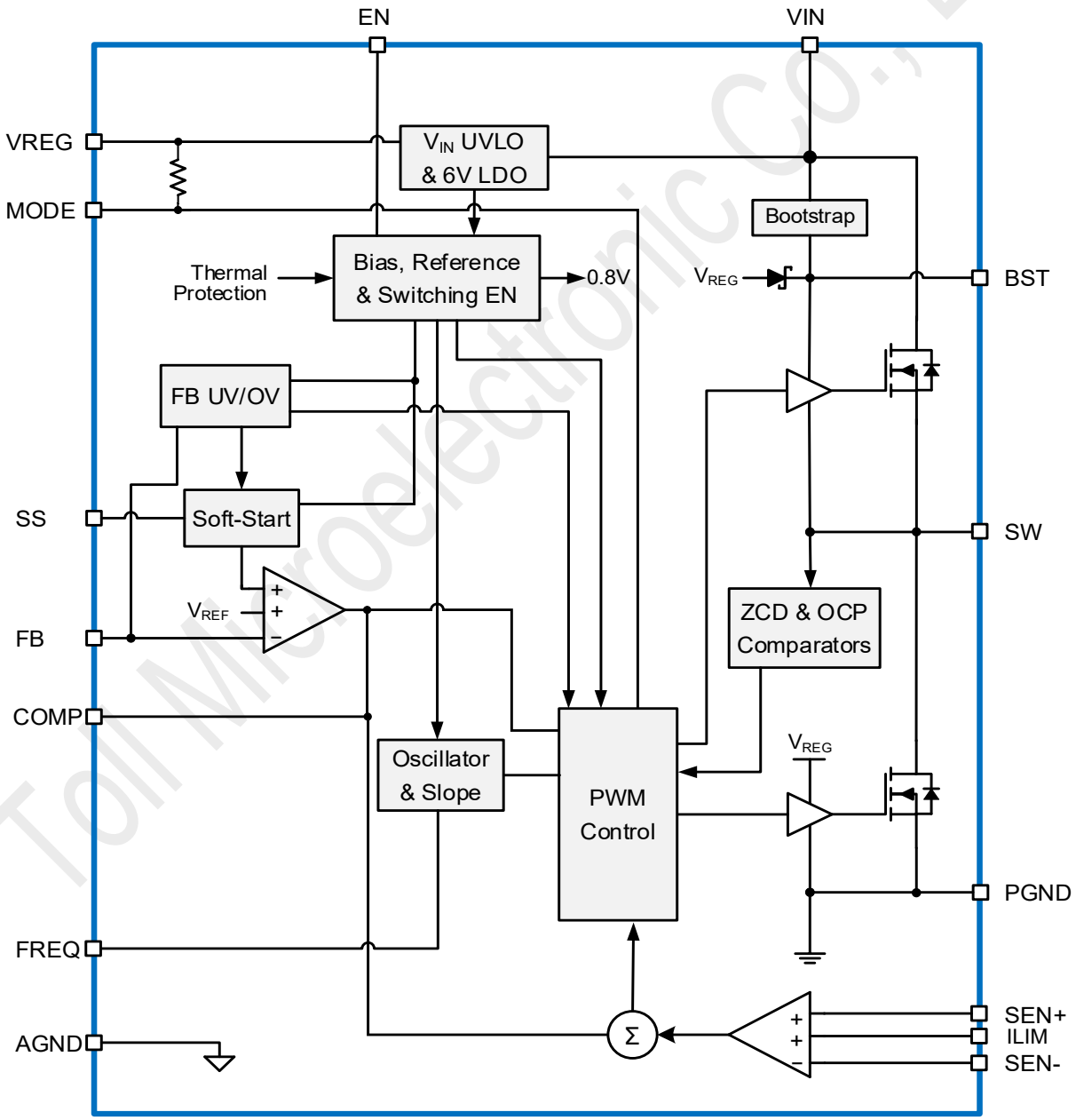


Figure 1. TMI3351 Block Diagram

8. Pin Description

Pin NO.	Pin Name	Description
1,2,3,4,5, 27,28, PAD1	VIN	Power supply input pin. Must bypass with a low ESR ceramic capacitor. Place cap as close to the IC as possible.
6	VREG	Output pin of the internal 6V bias regulator. Locally decouple to PGND using a low ESR/ESL capacitor located as close to the IC as possible.
7	EN	Enable control pin, logic high enable. This pin has an internal 1MΩ resistor to ground.
8,11,18, PAD2	AGND	Analog ground pin. It is internally connected to the sensitive analog ground circuitry. The exposed pad must be soldered to the PCB ground plane. It serves as a means of conducting heat way from the IC.
9	SS	Soft-Start control pin. This pin is used to program soft-start period with an external connect a capacitor. A 100nF is recommended from this pin to ground.
10	COMP	Output of the error amplifier, input to the PWM comparator. A RC network is connected from this pin to AGND to compensate the overall loop.
22,23,24	PGND	Power ground pin. The power ground copper needs to be connected to these pins.
12	FREQ	Switching frequency program pin. A resistor to ground sets the frequency from 100kHz to 1MHz.
13	MODE	Mode selection pin for light load. When this pin voltage is higher than 2.5V, the converter is set as PFM mode. This pin is internal resistor pulled up to VREG and can be left floating default for PFM operation. When the MODE pin is pulled to low, the forced continuous current mode is active.
14	FB	The Buck output feedback pin. Connect this pin to output through a resistor divider.
15	ILIM	Current program pin. A resistor to ground sets the peak current limit and average current limit.
16	SEN-	Negative input for the current sense. The sensed inductor current limit threshold is determined by voltage of ILIM pin.
17	SEN+	Positive input for the current sense. The sensed inductor current limit threshold is determined by voltage of ILIM pin.
19,20,21, 25, PAD3	SW	The Buck switching node pin.
26	BST	Buck high-side MOSFET M_T driver supply pin. Connect a 100nF capacitor (C_{BST}) and a 10Ω resistor between this pin and the SW pin.

9. Absolute Maximum Ratings[1]

Parameters		Symbol	Value
Maximum Input voltage		VIN, EN	32V
Voltage on pins with respect to ground		SW	-0.3V (-4V for <20ns) ~ 32V
		VREG	-0.3V to 6.5V
		BST	(V_{SW}–0.3V) to (V_{SW}+6.5V)
		SEN+, SEN-	-0.3V to 25V
		SS, COMP, ILIM, FREQ, MODE, FB	-0.3V to 6.5V
Maximum operating junction temperature[2]			+150ºC
Storage temperature			-55ºC to +150ºC
Thermal resistance of junction to case, θ_{JC}[3]			15 ºC/W
Thermal resistance of junction to ambient, θ_{JA}[3]			40 ºC/W
ESD[4]	All pads, according to human-body model, JEDEC STD 22, method A114		2kV
	According to charged-device model, JEDEC STD 22, method C101		500V

Note: *1. Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification are not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

2. Not to exceed the maximum junction temperature of the IC, which relate to the power consumption of the IC and the thermal resistance of the IC package. For a typical application (refer to the Block Diagram, Page 2), the power consumption of the IC comprises the operation power of the IC. The operation power of the IC can be calculated by $P_D=V_{IN}\times I_{IN}$, where V_{IN} represents the voltage at the VIN pin and I_{IN} represents the IC operation current of internal control and driver circuitry.

3. Measured on JESD51-7, 4-layer PCB

4. CAUTION: ESD sensitive device. Precaution should be used when handling the device in order to prevent permanent damage.

10. Recommended Operating Conditions

Parameter	Value
Input supply voltage	4V to 30V
Output voltage	0.8V to 30V
Operating ambient temperature range, T_A	-40ºC to +85ºC
Operating junction temperature range, T_J	-40ºC to +125ºC

11. Electrical Characteristics

All specifications below are at ambient 25ºC, V_{IN}= 5V to 30V, unless otherwise noted.

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
Supply Voltage (VIN Pin)						
V_{INON}	Turn-on threshold voltage	V_{IN} rising	3.6	4.0	4.25	V
V_{INOFF}	Turn-off threshold voltage	V_{IN} falling	3.3	3.5	3.75	
I_{SHDN}	VIN shutdown current	V_{IN} rising, V_{IN}=24V，V_{EN}=0V	–	–	5	μA
I_Q	VIN standby current	V_{IN}=24V, V_{FB}=2.0V, No switching	–	–	1.3	mA
6V Internal Regulator (VREG Pin)						
V_{REG}	6V internal regulator output voltage	I_{VREG}=1mA, V_{IN}≥7V,	5.7	6	6.3	V
		I_{VREG}=1mA, V_{IN}=4.0V	–	3.95	–	V
C_{VREG}	Output capacitor range		–	4.7	–	μF
Enable Logic Control (EN pins)						
V_{ENH}	Enable pins logic high (enabled)	When V_{ENH}≥1.2V, it is enabled;	1.2	–	–	V
V_{ENL}	Enable pins logic low (disabled)	When V_{ENH}≤0.4V, it is disabled.	–	–	0.4	
Internal Oscillator (FREQ pin)						
f_{SW_LOW}	Lowest switching frequency		–	–	100	kHz
f_{SW_HIGH}	Highest switching frequency		1000	–	–	kHz
f_{SW}	Operating frequency	R_{FREQ}=107kΩ	170	200	230	kHz
D_{MAX}	Maximum duty cycle		–	99.5	–	%
Error Amplifier						
V_{REF_FB}	Feedback reference voltage	T_J=25ºC	0.784	0.80	0.816	V
		T_J= -40ºC to 125ºC	0.776	0.80	0.824	
Soft-Start						
I_{SS}	Soft-start source current	SS = 0.8V	2	4	6	μA
Output Voltage Monitor						
V_{FB_OVP}	FB OVP rising threshold	FB pin, measured with respect to V_{REF}	115%	118%	122.5%	V_{REF}
V_{FB_ROVP}	OVP fault return threshold	FB pin, measured with respect to V_{REF}	–	102%	–	V_{REF}
Over-Current Limit (OCL)						
I_{OCL}	Cycle-by-cycle of inductor current limit	R_{ILIM} = 40kΩ, R_{FREQ}=87.6kΩ R_{SENSE}=7mΩ	–	10	–	A

11. Electrical Characteristics (Continued)

All specifications below are at ambient 25ºC, V_{IN}= 5V to 30V, unless otherwise noted.

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
Power MOSFET						
R_{MT}	High-side MOSFET static drain-source on-resistance		–	10	–	mΩ
R_{MB}	Low-side MOSFET static drain-source on-resistance		–	8	–	mΩ
Thermal Shutdown						
T_{SHDN}	Thermal shutdown trip threshold		–	160	–	ºC
ΔT_{SHDN}	Thermal shutdown hysteresis		–	20	–	

12. Operational Description

The TMI3351 is an integrates two low Rdson N-MOSFETs synchronous buck converter. The buck converter utilizes peak current mode control for instant transient response and easier compensation over the 4 to 30V supply range. There is an external soft-start, and a MODE pin to select between DCM mode and FCCM mode for light load condition. The TMI3351 also features include UVLO, OCP, OPP, OVP, SCP, TSDN.
Refer to Block Diagram for the following discussions. All parameters mentioned below are typical values.

12.1 Under-voltage Lockout

When VIN pin voltage is below the turn-on threshold, the device is held in a low power shutdown mode, drawing less than 5μA from the VIN pin. Once VIN is above the turn-on threshold, the internal bias rails and the VREG regulator are enabled. The PWM controller commences operation when the output of internal M_T bootstrap is established. A minimum hysteresis of 500mV on VIN pin provides hysteresis that prevents abnormal shutdown due to line voltage transient drop during power on period.

12.2 VREG Internal Regulator

The TMI3351 devices provide an internal 6V LDO using input from VIN. When V_{IN} exceeds 4.0V, the internal LDO regulator is enabled. The V_{REG} voltage provides bias voltage for the internal analog circuitry and also provides supply voltage for the gate drives.
For V_{IN} less than 6V, the V_{REG} tracks V_{IN} with a small voltage drop. The dropout voltage of VREG with 20mA load current is maximum 300mV when V_{IN}=4V.

12.3 Peak Current Mode Control with Slope Compensation

The TMI3351 implement peak current mode control. It provides fast transient response, cycle-by-cycle current limiting, and ease of loop compensation. The controller provides internal slope compensation to ensure stable operation with a duty cycle greater than 50%.

12.4 Operating Mode

TMI3351 works in forced PWM mode at connect MODE pin to GND. In FCCM condition, buck on-time is determined by internal circuit to get a constant switching frequency based on V_{IN}/V_{OUT} ratio. This forces inductor current works in continuous mode with constant frequency, can produce lower output voltage ripple, but the efficiency is low at light load condition because of the high switching loss.
It works in DCM mode at connect MODE pin to high than 2.5V. In DCM mode, the efficiency can be improved under light load condition, but the output voltage ripple will be larger than FCCM, it also works with constant switching frequency under heavy load condition, when the load is light or no-load, the controller will enter pulse skipping mode.

12.5 Synchronous MOSFET

The TMI3351 contains two internal NMOS switch. The gate driver circuit of high side MOSFET works in conjunction with an internal diode and an external bootstrap capacitor. A 100nF or larger ceramic capacitor, connected with short traces between the BST pin and SW pin is recommended. During the off-time of top-side MOSFET, the SW pin voltage is approximately 0V and the bootstrap capacitor charges from V_{REG} through the internal bootstrap diode. When operating with a high PWM duty cycle, the top-side switch will be forced off if it turns on time above maximum on time, to ensure that the bootstrap capacitor is recharged.
When TMI3351 commences operation from cold-start or wakes up from pulse-skipping mode, it will firstly turn on the bottom-side MOSFETs M_B，and last till both of the (BST-SW) voltage above 2.5V. This ensures that the

top-side MOSFETs M_T, gate driver power supply rail is sufficiently.

12.6 Soft-Start

The controller features a programable soft-start function, which reduces inrush current and overshoot of the output voltage. When the power on, the internal circuitry generates a soft-start voltage ramping up from 0V to VREG. When it is lower than the reference voltage, SS voltage overrides FB, so the error amplifier uses SS voltage as the reference. When SS voltage is higher than reference voltage, the reference regains control and enters close loop.

An external capacitor connected from SS to AGND is charged from an internal 4μA (typical) current source, producing a ramped voltage.

12.7 Maximum on duty improves dropout

When input voltage approaches the output voltage, the TMI3351 is designed to operate at top-side MOSFETs M_T maximum duty on mode to satisfy the duty cycle requirement to regulate the output voltage. If the input further drops to equal the output voltage, the TMI3351 forces the top-side MOSFETs M_T to remain on for more than one cycle, eventually reaching 99.5% duty cycle. In this low dropout mode, the controller turns on top-side MOSFETs M_T for multiple switching cycles until it turns off top-MOS switch momentarily and turns on bottom-MOS switch to refresh the BST supply voltage when the voltage of (BST-SW) is drops below 2.5V. In order to avoid the switching frequency entering the audio range, the minimum switching frequency is limited at 25kHz in low dropout mode.

12.8 Current Limit

The controller provides cycle-by-cycle current limit to protect against over-current conditions. The over-current limit (OCL) scheme senses the R_{SENSE} current. If the sensed current is larger than the I_{OCL}, an over current condition occurs. The present switching cycle is terminated (cycle-by-cycle current limit), and the MOSFETs M_T is turned off immediately. the MOSFETs M_T cannot be turned on again until the inductor current drops to the valley current limit.

If the Soft-start is completed and the FB is less than 54% V_{REF}, an V_{OUT} short condition occurs. the MOSFETs M_T and M_B are turned off immediately. Then the IC enter the hiccup mode to periodically restart the part. Meanwhile, the frequency would be lowered when FB < 350mV, maximum frequency conversion ratio is 1/2. This protection mode is especially useful when the output is dead-shorted to ground. The average short-circuit current is greatly reduced to alleviate the thermal issues. The TMI3351 exits the hiccup mode once the over-current condition is removed.

12.9 V_{OUT} cable impedance compensation

V_{OUT} has a cable drop compensation. The slope is a default value that can be set by the factory. If external feedback resistor is applied, R_{FB1} must be 100kΩ and R_{SENSE} must be 7mΩ to have the designed slope.

$$V_{CAB\_COMP} = \frac{R_{FB1}(\Omega) \times R_{sense}(\Omega) \times I_{OUT}}{700} \times CABLE\_COMP$$

Where R_{FB1} is the upper resistor of the feedback divider network. R_{SENSE} is current sense resistor value to sense output current. CABLE_COMP is 0mΩ(default), 20mΩ, 40mΩ, 60mΩ four gears can be selected and set by the factory.

The typical values of the R_{SENSE} is 7mΩ.

For example, R_{FB1} = 100kΩ, R_{SENSE} = 7mΩ, I_{OUT} = 1A, set CABLE_COMP = 20mΩ, V_{OUT} cable impedance compensation voltage is:

$$V_{CAB\_COMP} = \frac{100 \times 10^3 \times 7 \times 10^{-3} \times 1A}{700} \times 20m\Omega = 20mV$$

12.10 Over-Voltage Protection (OVP)

When the voltage at the FB pin (V_{FB}) is 18% above the feedback reference voltage V_{REF}, an output OVP fault is set. All of the switches will be turned off, and discharge circuit starts to discharge output through SW pin. Switching resumes once the output falls down to 102% of V_{REF}.

12.11 Thermal Shutdown (TSDN)

The TMI3351 also has a built-in thermal shutdown circuit that prevents heat damage to the IC. Normal operation should always be within the IC's power dissipation rating. If the rating is exceeded for a continued period, the junction temperature T_J will rise above 160ºC and will activate the TSDN circuit. It will turn off the M_T & M_B switch. The device automatically restarts once the junction temperature drops by the thermal shutdown hysteresis of 20ºC below the thermal shutdown threshold.

13. Application Information

13.1 Setting the Output Voltage

Output voltage can be set by feeding the output back to the FB pin with a resistor divider network.

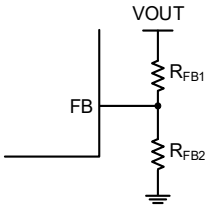


Figure 2. VOUT Setting Resistor

As shown in Figure 2, the resistor divider network includes R_{FB1} and R_{FB2}. Usually, first is picking a fixed R_{FB1} value (such as 100kΩ) then using the equation below to calculate the R_{FB2} value:

$$R_{FB2} = \frac{0.8 \times R_{FB1}}{V_{OUT} - 0.8}$$

Some of the normally used output voltages and corresponding R_{FB1} and R_{FB2} values are listed in the table below:

Table 1. Resistor Selection for Common Output Voltage

R_{FB1}(kΩ)	R_{FB2}(kΩ)	V_{OUT}(V)
100	18.7	5.0
113	11	9.0
113	8.06	12
113	6.34	15
113	4.7	20

13.2 Setting the Frequency

The selection of switching frequency is a trade-off between efficiency and component size. Low frequency operation increases efficiency by reducing MOSFET switching losses, but requires larger inductance and/or capacitance to maintain low output ripple voltage. The switching frequency of the TMI3351's controllers can be selected using the FREQ pin. The FREQ pin can be used to adjust the controller's operating frequency from 100kHz to 1MHz. The value of R_{FREQ} for a given operating frequency can be calculated by:

$$R_{FREQ}(k\Omega) = \frac{21800}{f_s(kHz)} - 4$$

To get f_s = 500kHz, set R_{FREQ} to 39kΩ.

Some recommended values of R_{FREQ} for most commonly used switching frequency are listed in Table 2.

Table 2. Frequency vs. R_{FREQ}

R_{FREQ} (kΩ)	Frequency (kHz)
150	150
68	300
39	500
18	1000

The PWM switching frequency is programmable, while the duty cycle is fixed limited to 99.5%, allowing the bootstrap capacitor to charge during when the voltage is low. The TMI3351 allows a high ratio of input to output voltage conversion.

13.3 Setting the Peak Current Limit

The peak current limit can be set with below formula.

$$I_{PEAK}(A) = \frac{R_{ILIM}(k\Omega)}{6.5 * R_{FREQ}(k\Omega) * R_{SENSE}(\Omega)}$$

Where R_{SENSE} is current sense resistor value to sense output current, R_{ILIM} is resistor at ILIM pin, R_{FREQ} is resistor at FREQ pin.

The typical values of the R_{SENSE} is 7mΩ.

13.4 Setting the Average Current Limit

The value of average current limit can be calculated by following formula.

$$I_{AVG} = 60\% \times I_{PEAK}$$

The threshold calculated by the above formula is the value when internal average current limit signal is pulled low, the actual value will be higher.

13.5 Input Capacitor Selection

The input current of a buck convertor is discontinuous, therefore an input capacitor must be connected between the Vin pin and GND pin to keep the input voltage stable and filter out the pulsing input current.

The voltage rating of input capacitor must be greater than maximum input voltage plus ripple voltage. The input ripple voltage can be approximated by equation below:

$$\Delta V_{IN} = \frac{I_{OUT}}{f_S \times C_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times \frac{V_{OUT}}{V_{IN}}$$

As mentioned above, the input current is discontinuous in a buck converter, the current stress on the input capacitor is necessary to concern when selecting the capacitor. For a buck circuit, the RMS value of input capacitor current can be calculated by:

$$I_{CIN\_RMS} = I_{OUT} \times \sqrt{\frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)}$$

According to the formula, it can be concluded that the I_{CIN_RMS} = 0.5 x I_{OUT} when V_{OUT} = 0.5 x V_{IN}, which is the worst case. To obtain the best performance and reliability, the input capacitors must have current rating higher than I_{CIN_RMS} at worst operating conditions. It should be noted that the ripple current rating from capacitor manufactures is based on certain amount of life time, so further de-rating needs to be considered for long term reliability.

Ceramic capacitor is the optimal choice for an input capacitor due to its low ESR and high ripple current rating. The X5R or X7R type dielectric ceramic capacitors are recommended for their better temperature and voltage characteristics. Depending on the application condition, other low ESR tantalum capacitor or aluminum electrolytic capacitor may also be suitable.

13.6 Inductor Selection

When a switching voltage is applied on an inductor, the inductor can provide the output with a constant current. The inductance can be calculated as follows:

$$L = \frac{V_{OUT}}{f_S \times \Delta I_L} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)$$

Higher inductance gives lower inductor ripple current and lower ripple voltage on the load, but leads to larger size of the inductor to avoid saturation. Low ripple current reduces inductor core losses. It also reduces RMS current through inductor and switches, which results in less conduction loss. Usually, the ripple current is recommended to be set to 30% of the maximum load current.

When selecting the inductor, make sure it is able to handle the peak current without saturation even at the highest operating temperature. The peak inductor current can be calculated as follows:

$$I_{LPEAK} = I_{OUT} + \frac{V_{OUT}}{2 \times f_S \times L} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)$$

The inductor takes the highest current in a buck regulation circuit. The conduction loss on the inductor should be taken in to account for thermal and efficiency requirements.

Shielded inductors are small and radiate less EMI noise, but at the cost of higher price than unshielded inductors. So, the selection of inductor depends on the trade-offs among EMI requirement, price and size.

13.7 Output Capacitor Selection

The output capacitor is used to provide the load with constant and stable voltage. The output capacitor is selected based on the DC output voltage rating, output ripple voltage specification and ripple current rating.

The selected output capacitor must have a higher rated voltage specification than the maximum desired output voltage including ripple. De-rating needs to be considered for long term reliability.

In a buck converter circuit, output ripple voltage is determined by inductor value, switching frequency, output capacitor value and ESR. It can be calculated by the equation below:

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_S \times L} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times \left(R_{ESR} + \frac{1}{8 \times f_S \times C_{OUT}}\right)$$

Where, C_{OUT} is output capacitor value and R_{ESR} is the Equivalent Series Resistor of output capacitor.

When low ESR ceramic capacitor is adopted for output capacitor, the output ripple voltage is determined by the output capacitor value and the inductor ripple current, and it can be calculated by using the equation below:

$$\Delta V_{OUT} = \frac{V_{OUT}}{8 \times {f_S}^2 \times L \times C_{OUT}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)$$

When tantalum capacitor or aluminum electrolytic capacitor is adopted for output capacitor, the impedance of ESR at switching frequency dominates, and it can be calculated by using the equation below:

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_S \times L} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times R_{ESR}$$

The X5R and X7R dielectric type of ceramic or other low ESR tantalum or aluminum electrolytic capacitors is suitable for low output ripple voltage requirement over the entire operational temperature range.

In a buck converter, output capacitor current is continuous. The RMS current of output capacitor is decided by the peak to peak inductor ripple current. It can be calculated by:

$$I_{Co\_RMS} = \frac{\Delta I_L}{\sqrt{12}}$$

Usually, the ripple current rating of the output capacitor is a less important issue than that of the input capacitor, due to its comparatively smaller current stress. It should be noted that the output capacitor could be overstressed when the inductor value is selected to be very small.

The output capacitor has some effects on the loop stability, the TMI3351 is optimized for wide range of output capacitor values and ESR ratings.

13.8 PCB Layout Considerations

All switching power supplies, especially for those with high switching frequency and high load currents, good PCB is crucial. A badly PCB layout might cause instability and noise issue. To maximize efficiency, switch rise and fall time are very fast. To prevent radiation of high frequency noise (for example, EMI), proper layout of the high-frequency switching path is essential.

In the TMI3351 buck regulator circuit, high pulsing current flows through two circuit loops. The first loop starts from the input capacitors, to Vin pin, to the filter inductor, to the output capacitor and load, and then return to the input capacitor through ground. Current flows in the first loop when the high side switch is on. The second loop starts from inductor, to the output capacitors and load, to the PGND pin, to SW pin. Current flows in the second loop when the low side switch is on.

In PCB layout, minimizing the two loops area reduces the noise of this circuit and improves efficiency. A ground plane is recommended to connect input capacitor, output capacitor, and PGND pin of the low-side switch.

Some layout tips for optimal electrical and thermal performance:

1. The input capacitor should be connected to the VIN pin (1~5, 27, 28) and the PGND pin (22~24) as close as possible.
2. The 22-24 pin is the power ground, and the power ground copper needs to be connected to these pins. The GND of PAD2 can drill several more vias on the power ground of the bottom layer. The GND of pins 8, 11 and 18 can be directly connected with GND of PAD2.
3. C_{BST} capacitor should be placed near the chip, and be connected to the BST pin and SW pin with short and thick wire.
4. Make the current trace from SW pin to L to C_{OUT} to the PGND pin as short as possible. Meanwhile, the current trace from in input capacitor to VIN pin, then to the PGND pin should be kept as short as possible to reduce the EM radiation.
5. Place the feedback resistors as close to the FB pin as possible, the trace from FB pin to AGND as short as possible.
6. Keep sensitive signal trace such as trace connected with FB pin, COMP pin, FREQ pin, ILIM pin far away from the SW trace.
7. Route the sensing traces (SEN+, SEN-) in paired way with smallest closed area. Avoid crossing noisy areas such as SW. Place the RC filter for the current sense signal as close to the IC pins as possible. At the same time, a short and wide type resistor is recommended for current sense. When the output voltage is greater than or equal to 24V, the current sense resistor needs to be placed on the low side. When the output voltage is less than 24V, the current sense resistor can be placed on the high side in order to lay the ground wire more conveniently.
8. VREG capacitor should be placed as close as possible to VREG pin. The capacitor ground needs to be connected to the GND of PAD2 as short as possible.

9. The ground return of input/output capacitor should be tied close with large PGND copper area.
10. For heavy load, suggest layout large copper, more layers and more vias for heat sink to enhance the thermal performance.

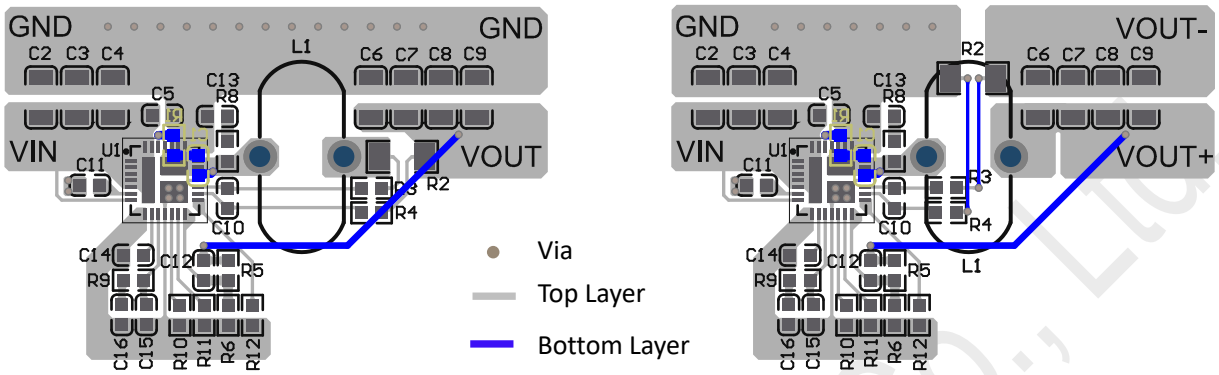


Figure 4. Layout Recommendation

14. Typical Application Schematic:

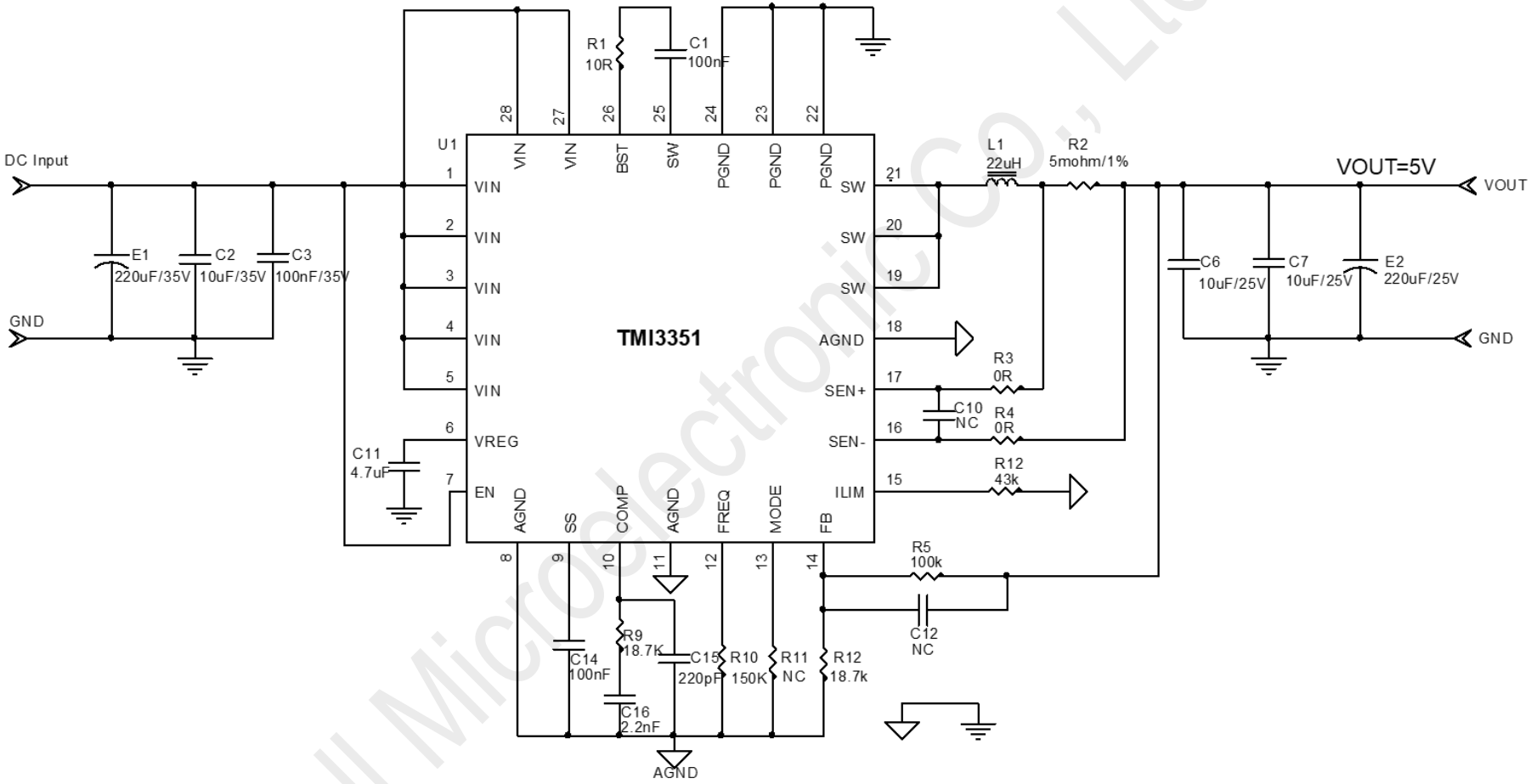


Figure 5. Typical Application Schematic with High Side Current Sense (V_{OUT}<24V)

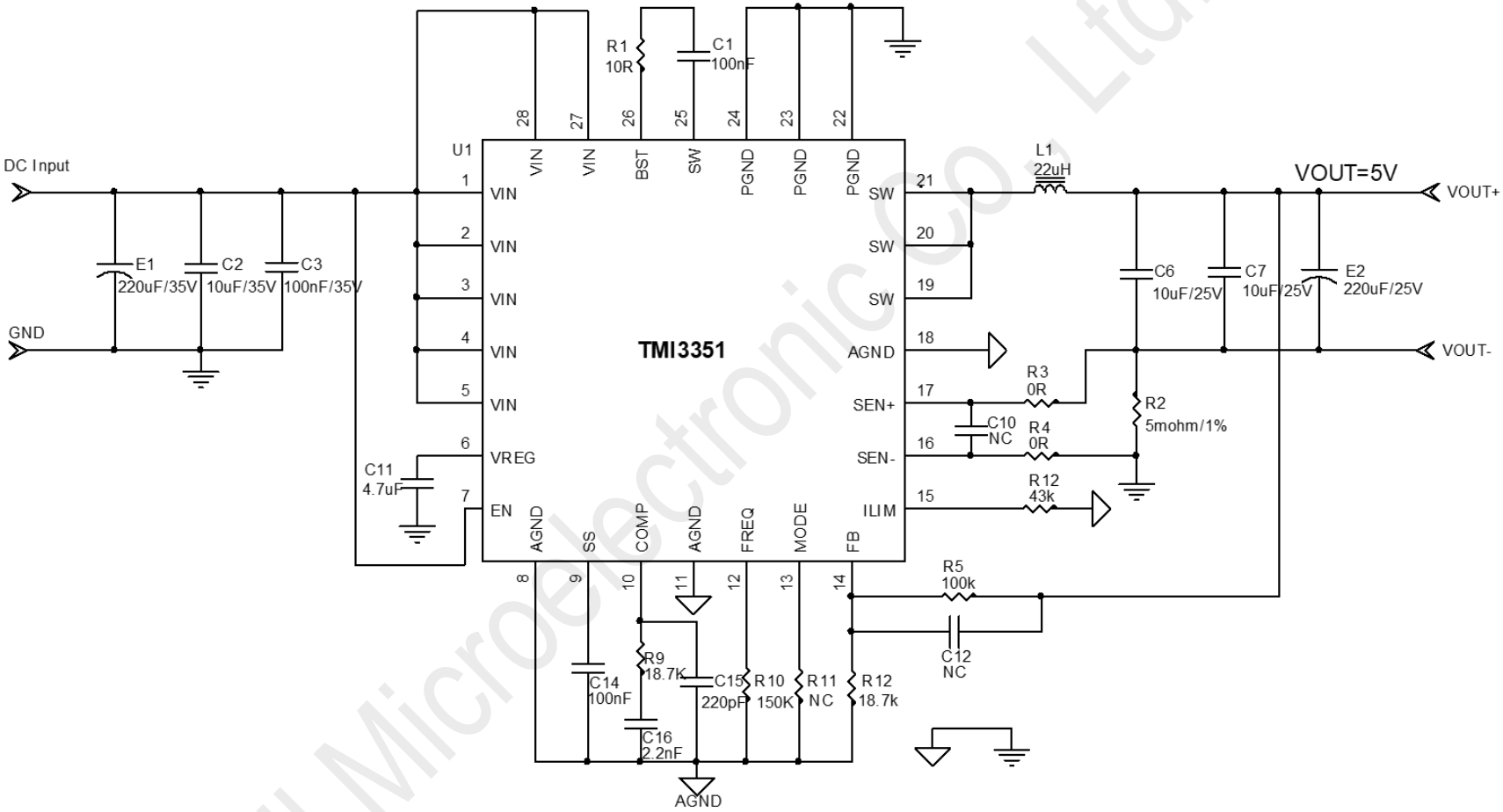
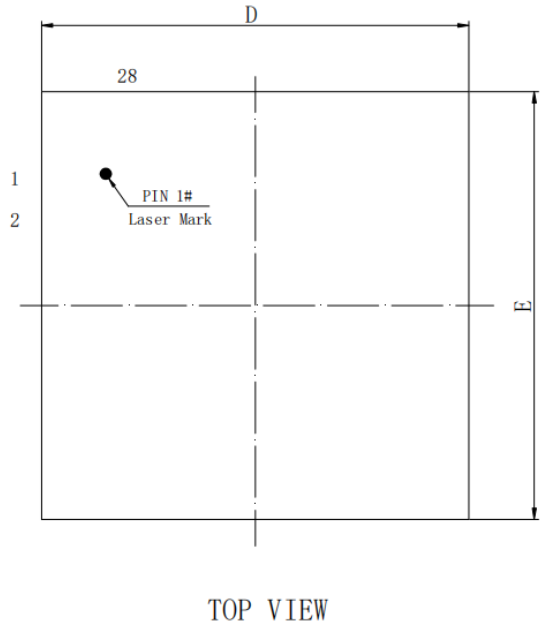
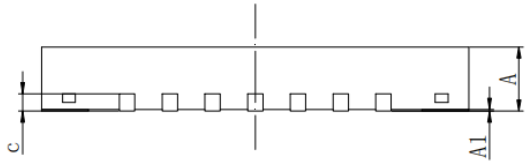


Figure 6. Typical Application Schematic with Low Side Current Sense (V_{OUT}≥24V)

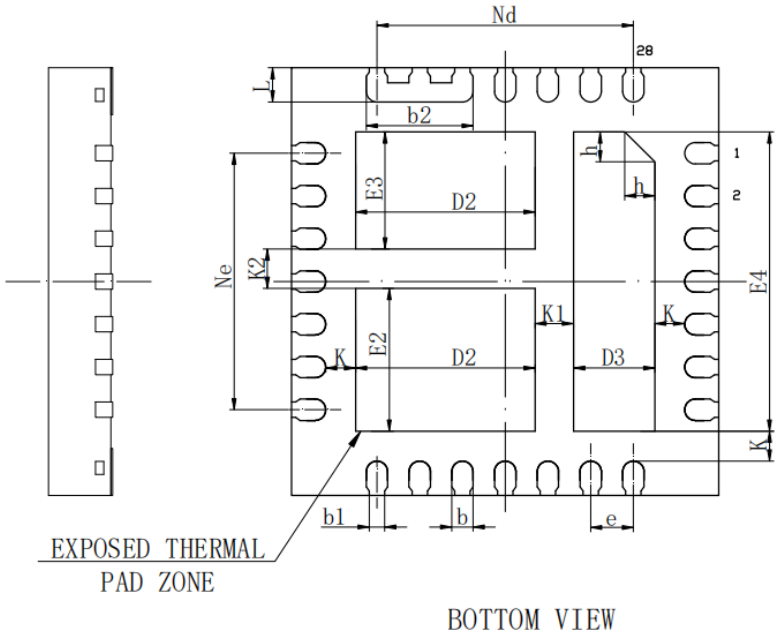
15. Package Information: QFN-28, 5mm×5mm×0.75mm



TOP VIEW



SIDE VIEW



BOTTOM VIEW

SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	0	0.02	0.05
b	0.20	0.25	0.30
b1	0.18REF		
b2	1.20	1.25	1.30
c	0.203REF		
D	4.90	5.00	5.10
D2	2.00	2.10	2.20
D3	0.85	0.95	1.05
e	0.50BSC		
Nd	3.00BSC		
Ne	3.00BSC		
E	4.90	5.00	5.10
E2	1.57	1.67	1.77
E3	1.27	1.37	1.47
E4	3.40	3.50	3.60
L	0.35	0.40	0.45
h	0.30	0.35	0.40
K	0.35REF		
K1	0.45REF		
K2	0.46REF		

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