

Dual Channel Time-to-Digital Converters for Time-of-Flight

Applications in LIDAR, Range Finders, and ADAS

1. FEATURES

- Typical time resolution: 38ps
- Standard Deviation:
 - 10ps (Mode 1, 100ns)
 - 50ps (Mode 2, 10μs)
- Measurement Range:
 - Mode 1: 3ns to 1000ns
 - Mode 2: 250ns to 8ms
 - Mode 3: 0ns to 1000ns (with inner delay compensation for dead time)
 - Mode 4: 250ns to 250ms
- Support up to 5 STOP Signals for each TDC
- Autonomous Multi-Cycle Averaging Mode, up to 128 Sampling Average and Save Host Controller Power
- Support SPI Interface and Multiple Register Accessible
- Power Supply: 2.2V to 3.6V
- Low Current Consumption in Standby Mode with 200μA for each TDC
- Operating Temperature: -40°C to 125°C
- Package: FBGA4x4-25

2. APPLICATION

- Ultrasonic meter: Gas Meter, Water Meter.
- Time of Flight measurement in SONAR, LIDAR, Drones, Robot Vacuum Cleaner.
- Displacement Sensing.
- Collision Detection Systems
- Biomedical Engineering Instruments, PET-CT Image, Fluorescence-lifetime-image.

3. GENERAL DESCRIPTION

The TMIS7702 is a two-channel time to digital converters (TDC). It performs the function of a stopwatch and measures the elapsed picoseconds to microseconds between a START pulse and up to five STOP pulses. The ability to measure from START to multiple STOPS gives users the flexibility to select which STOP pulse yields the best echo performance. The device has an internal self-calibrated time base which compensates for drift over time and temperature. Self-calibration enables time-to-digital conversion accuracy in the order of picoseconds. The high time resolution and accuracy make TMIS7702 ideal for time-of-flight sensing, such as in centimeter accuracy LIDAR application and ultrasonic flow metering. TMIS7702 can work in the Autonomous Multi-Cycle Averaging Mode. In this mode, the host can go to sleep to save power, and it can wake up when interrupted by the TDC upon completion of the measurement sequence. This working mode is optimized for low system power consumption, making it ideal for battery powered flow meters.

4. TYPICAL APPLICATION

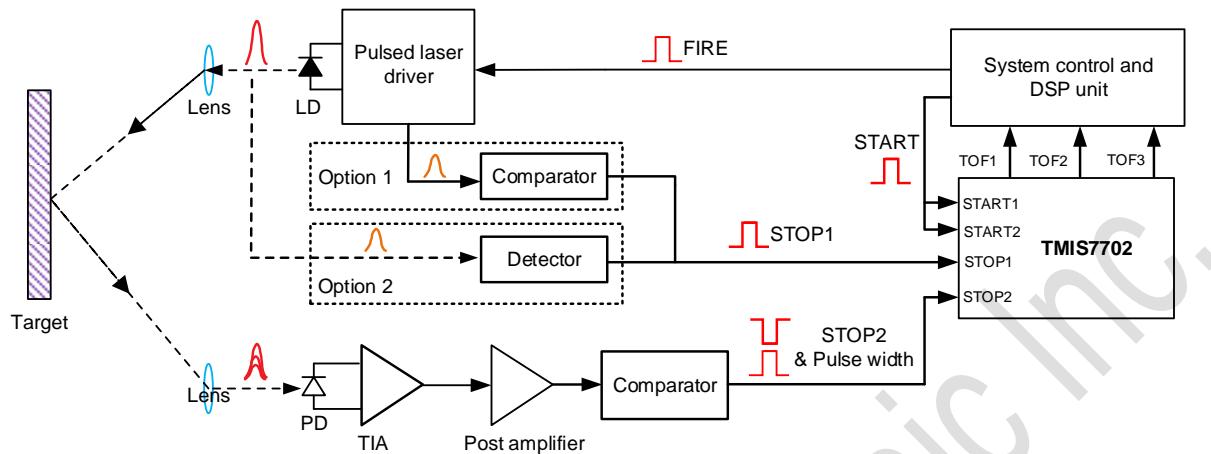
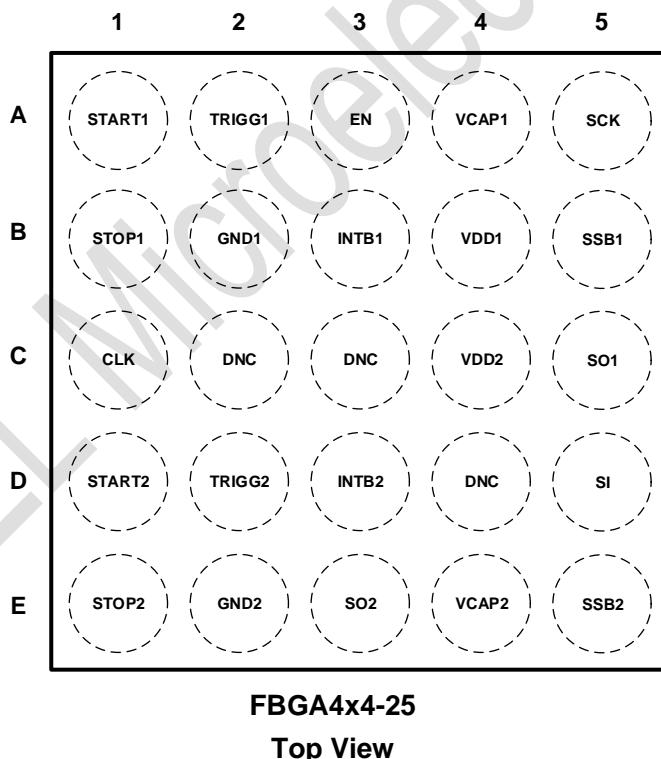


Figure 1. Application Circuit Example in LIDAR

5. Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Unit
VDD	Low-voltage digital supply	-0.3	3.9	V
VI	Terminal Input voltage	-0.3	VDD+0.3	V
V _{DIFF_IN}	Voltage differential between any two input terminals		3.9	V
V _{IN_GND_VDD}	Voltage differential between input terminals between GND and VDD		3.9	V
I _{IN}	Input current at any pin	-5	5	mA
T _A	Ambient operating temperature	-40	125	°C
T _{stg}	Storage temperature	-40	150	°C

6. PIN CONFIGURATION



Top Mark: TMIS7702/XXXXX (TMIS7702: Device Code, XXXXX: Inside Code)

Part Number	Package	Top mark	Quantity/Tray
TMIS7702	FBGA4x4-25	T7702 XXXXX	490

TMIS7702 devices are Pb-free and RoHS compliant.

7. PIN FUNCTIONS

Pin	Name	Type	Function
A1	START1	Input	START signal of TDC1
A2	TRIGG1	Output	Trigger output signal of TDC1
A3	EN	Input	Input enable signal to TDC
A4	VCAP1	Output	LDO output terminal for external decoupling cap
A5	SCK	Input	SPI clock
B1	STOP1	Input	STOP signal for TDC1
B2	GND1	Ground	Ground
B3	INTB1	Output	Interrupt to MCU for TDC1
B4	VDD1	Power	Supply input
B5	SSB1	Input	SPI chip selection for TDC1, Active low
C1	CLK	Input	Clock input to TDC
C2	NC	-	No connect
C3	NC	-	No connect
C4	VDD2	Power	Supply input
C5	SO1	Output	SPI data output for TDC1
D1	START2	INPUT	START signal of TDC2
D2	TRIGG2	Output	Trigger output signal of TDC2
D3	INTB2	Output	Interrupt to MCU for TDC2
D4	NC	-	No connect
D5	DIN	Input	SPI data input
E1	STOP2	Input	STOP signal for TDC2
E2	GND2	Ground	Ground
E3	SO2	Output	SPI data output for TDC2
E4	VCAP2	Output	LDO output terminal for external decoupling cap
E5	SSB2	Input	SPI chip selection for TDC2. Active low

8. ESD RATING

Items	Description	Value	Unit
V_{ESD_HBM}	Human Body Model for all pins	± 4000	V
V_{ESD_CDM}	Charged Device Model for all pins	± 1000	V

JEDEC specification JS-002

9. Recommended Operating Conditions

$T_A = 25^\circ\text{C}$, $V_{DD1}=V_{DD2} = 3.3\text{V}$ (unless otherwise noted).

Parameter	Test Conditions	Min	TYP	Max	Unit
V_{DD}	Supply voltage	2.2		3.6	V
VI	Terminal voltage	0		V_{DD}	V
VIH	Voltage input high	$0.7 \times V_{DD}$		3.6	V
VIL	Voltage input low	0		$0.3 \times V_{DD}$	V
F_{CALIB_CLK}	Frequency (Reference or Calibration Clock)	1	8	16	MHz
T_{CLOCK}	Time period (Reference or Calibration clock)	62.5	125	1000	ns
$DUTY_{CLOCK}$	Input clock duty cycle		50		%

Timing Requirements: Measurement Mode 1

$T_{1STARTSTOP_Min}$	Minimum Time between Start and Stop Signal	3			ns
$T_{1STOPSTOP_Min}$	Minimum Time between 2 Stop Signals	50			ns
$T_{1STARTSTOP_MAX}$	Maximum Time between Start and Stop Signals		1500		ns
$T_{1STOPSTOP_MAX}$	Maximum Time between Stop and Stop Signals		1500		ns

Timing Requirements: Measurement Mode 2

$T_{2STARTSTOP_Min}$	Minimum Time between Start and Stop Signal	$2 \times t_{CLOCK}$			s
$T_{2STOPSTOP_Min}$	Minimum Time between Stop and Stop Signal	$2 \times t_{CLOCK}$			s
$T_{2STARTSTOP_Max}$	Maximum Time between Start and Stop Signal			$(2^{16}-2) \times t_{CLOCK}$	s
$T_{2STOPSTOP_Max}$	Maximum Time between Stop and Stop Signal			$(2^{16}-2) \times t_{CLOCK}$	s

Timing Requirements: Enable Input

T_{REN}	Rise Time for Enable Signal (20%-80%)	2		200	ns
T_{FEN}	Fall Time for Enable Signal (20%-80%)	2		200	ns

Timing Requirements: START, STOP, CLK

T_{RST}, T_{FST}	Maximum rise, fall time for START, STOP signals (20%- 80%)		2		ns
T_{RXCLK}, T_{FXCLK}	Maximum rise, fall time for external CLOCK (20%-80%)		2		ns

Timing Requirements: TRIGG

$T_{TRIGSTART}$	Time from TRIG to START			6	ns
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Temperature

T_A	Ambient temperature	-40		125	°C
T_J	Junction temperature	-40		125	°C

10.Thermal Information

Items	Description	Value	Unit
θ_{JA}	Junction-to-ambient thermal resistance	155	°C/W
$\theta_{JC(\text{top})}$	Junction-to-case (top) thermal resistance	109	°C/W
θ_{JB}	Junction-to-board thermal resistance	114	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	20	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	110	°C/W

11.Electrical Characteristics

PARAMETER	TEST CONDITIONS	Min	TYP	Max	Unit
TDC Characteristics					
LSB	Single shot measurement	38			ps
T _{ACC-2} Accuracy Mode 2	CLK = 8 MHz	25			ps
T _{STD-2} Standard Deviation Mode 2	Measured Time = 200μs Measured Time = 2μs	50			ps
Output Characteristics: TRIGGx, INTBx, SOx					
V _{OH} Output voltage high	I _{source} = -2 mA	2.32	2.95		V
V _{OL} Output voltage low	I _{sink} = 2 mA	0.35	0.99		V
Input Characteristics: EN, STARTx, STOPx, CLK, SI, SSBx, SCK					
C _{in} Input capacitance			3		pF
Power Consumption					
I _{SD} Shutdown current	EN = LOW	0.1			μA
I _{QA} Quiescent Current A	EN=HIGH, TDC running	3			mA
I _{QB} Quiescent Current B	EN=HIGH, TDC OFF, Clock Counter running	500			μA
I _{QC} Quiescent Current C	EN = HIGH; measurement stopped, SPI communication only	600			μA
I _{QD} Quiescent Current D	EN = HIGH, TDC OFF, counter stopped, no communication	400			μA

12.Timing Requirements

PARAMETER		MIN	TYP	MAX	UNIT
Timing Requirements: START1, STOP1, START2, STOP2, CLOCK					
PW _{START}	Pulse width for START signal	10			ns
PW _{STOP}	Pulse width for STOP signal	10			ns
Serial Interface Timing Characteristics (VDD=3.3V, f_{SCK}=25MHz)					
f _{SCK}	SCK frequency			25	MHz
t ₁	SCK period	40			ns
Serial Interface Timing Characteristics (VDD=3.3V, f_{SCK}=20MHz)					
t ₁	SCK period	50			ns
t ₂	SCK high time	16			ns
t ₃	SCK low time	16			ns
t ₄	SI setup time	5			ns
t ₅	SI hold time	5			ns
t ₆	SSB1 or SSB2 fall to SCK rise	6			ns
t ₇	Last SCK rising edge to SSB1 or SSB2 rising edge	6			ns
t ₈	Minimum pause time (SSBx high)	40			ns
t ₉	CLK fall to SO1 and SO2 bus transient			12	ns
Wake Up Time					
t _{Wakeup_period}	Time to be ready for measurement		300		μs

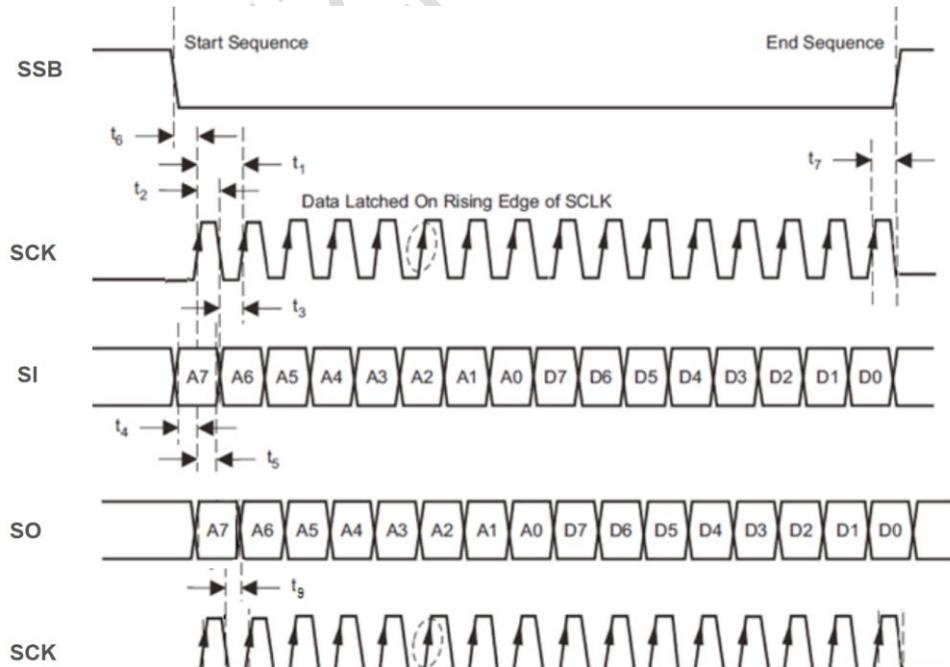


Figure 2. SPI Register Write: 8 bit Register Example

13.Detailed Description

Overview

TMIS7702 performs time measurement when START edge is asserted, and multiple subsequent measurements could be achieved when valid STOP edge is captured. The internal high precision time base can help measure time with accuracy in the order of picoseconds, this feature makes TMIS7702 ideal for wide application, such as LIDAR, flow meter.

Calculation Time-of-Flight (TOF)

With measurement mode 1, The TOF between the START to the nth STOP can be calculated using the below equation:

$$\text{normLSB} = \frac{T_{\text{OSC_PERIOD}}}{\text{calCount}} \quad \text{calCount} = \frac{\text{CALIBRATION2}-\text{CALIBRATION1}}{\text{CALIBRATION2}_{\text{PERIODS}}-1}$$

$$\text{TOF}_n = \text{TIME}_n \times \text{normLSB} + T_{\text{offset}}$$

Where:

- TOF_n [sec] = time-of-flight measurement from the START to the nth STOP
- TIME_n = nth TIME measurement given by the TIME1 to TIME6 registers
- normLSB [sec] = normalized LSB value from calibration
- CLOCKperiod [sec] = external CLOCK period
- CALIBRATION1 [count] = TDC count for first calibration cycle
- CALIBRATION2 [count] = TDC count for second calibration cycle
- CALIBRATION2_PERIODS = setting for the second calibration cycle; located in register TDCx_CONFIG2

With measurement mode 2, The TOF between the START to the nth STOP can be calculated using the below equation:

$$\text{TOF}_n = \text{normLSB} \times (\text{TIME1}-\text{TIME}_{n+1}) + \text{CLKCOUNT}_n \times T_{\text{OSC_PERIOD}}$$

$$\text{normLSB} = \frac{T_{\text{OSC_PERIOD}}}{\text{calCount}} \quad \text{calCount} = \frac{\text{CALIBRATION2}-\text{CALIBRATION1}}{\text{CALIBRATION2}_{\text{PERIODS}}-1}$$

Where:

- TOF_n [sec] = time-of-flight measurement from the START to the n th STOP
- TIME1 = TDCx_TIME1 register value = time 1 measurement given by the TMIS7702 register address 0x10.
- TIME_(n+1) = TDCx_TIME_(n+1) register value = (n+1) time measurement, where n = 1 to 5 (TDCx_TIME2 to TDCx_TIME6 registers).
- normLSB [sec] = normalized LSB value from calibration.
- CLOCK_COUNT_n = nth clock count, where n = 1 to 5 (TDCx_CLOCK_COUNT1 to TDCx_CLOCK_COUNT5).
- CLOCKperiod [sec] = external CLOCK period.
- CALIBRATION1 = TDCx_CALIBRATION1 register value = TDC count for first calibration cycle.
- CALIBRATION2 = TDCx_CALIBRATION2 register value = TDC count for second calibration cycle.

- CALIBRATION2_PERIODS = setting for the second calibration; located in register TDCx_CONFIG2.

TOLL Microelectronic Inc.

14.Functional Block Diagram

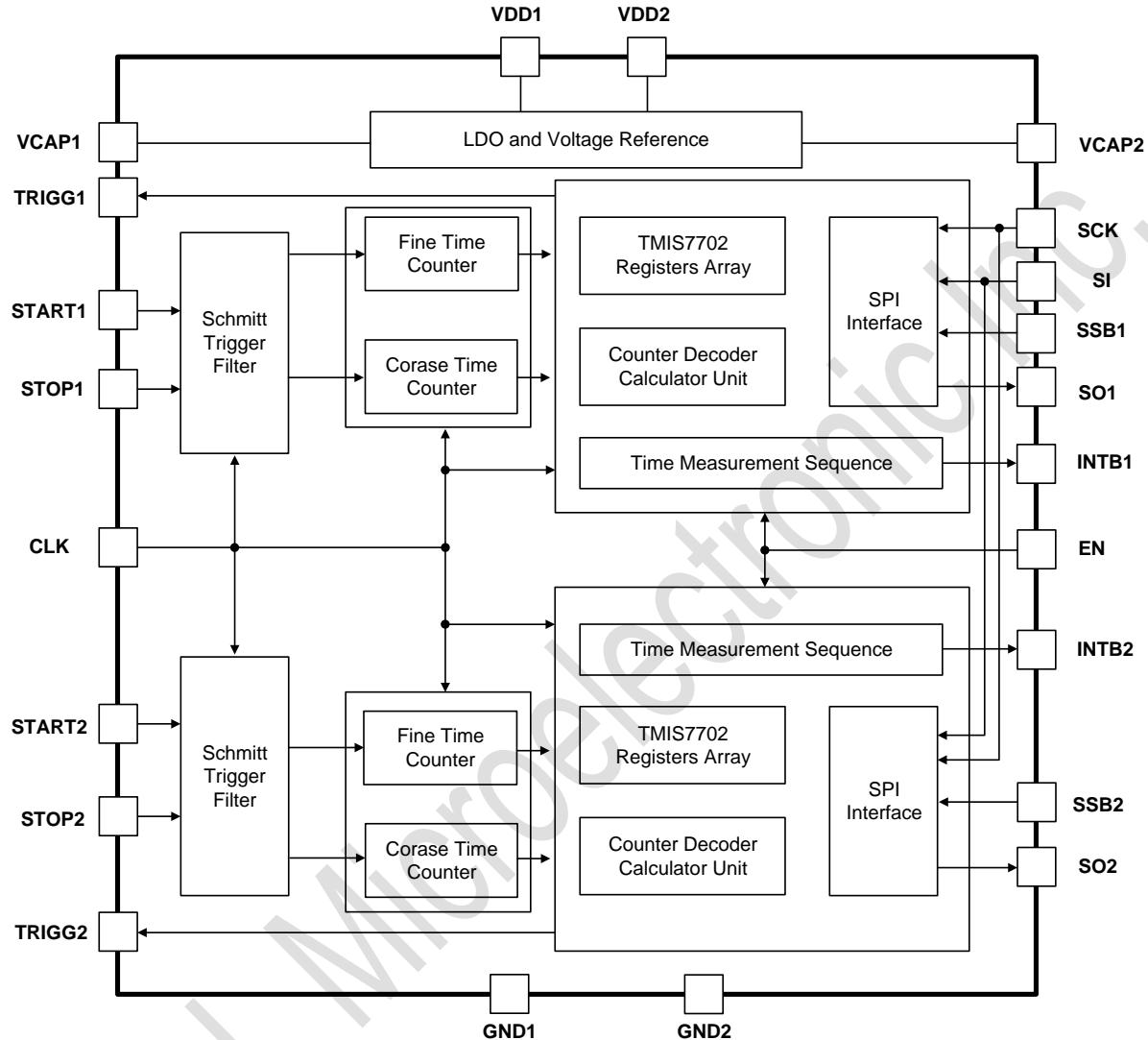


Figure 3. TMIS7702 Function Block Diagram

15. Typical Characteristics

VDD = 3.3 V, GND = 0 V, CLOCK = 8 MHz, CALIBRATION2_PERIODS = 10, AVG_CYCLES = 1, one STOP signal.

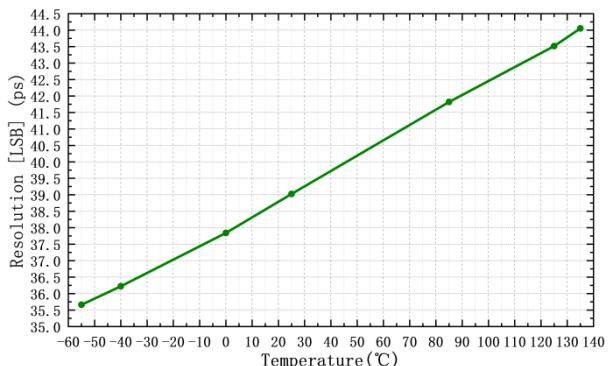


Figure 4. Resolution (LSB) vs. Temperature

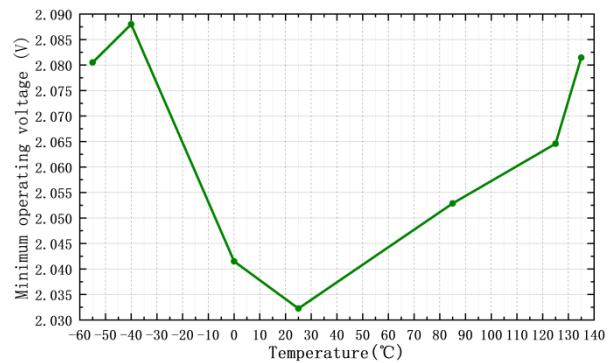


Figure 5. Minimum Operation Voltage vs. Temperature

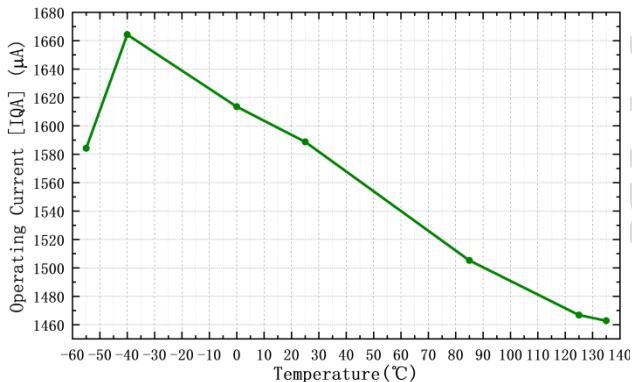


Figure 6. Operating Current (IQA) vs. Temperature

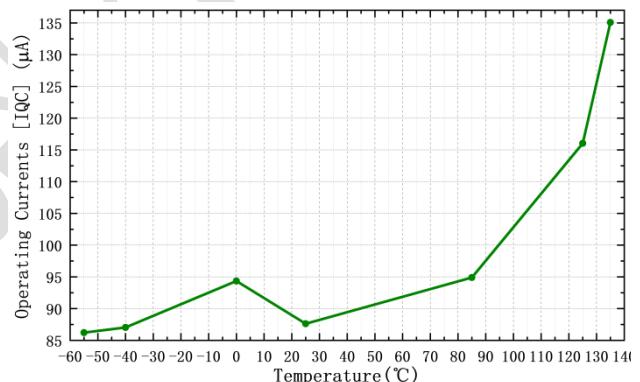


Figure 7. Operating Current (IQC) vs. Temperature

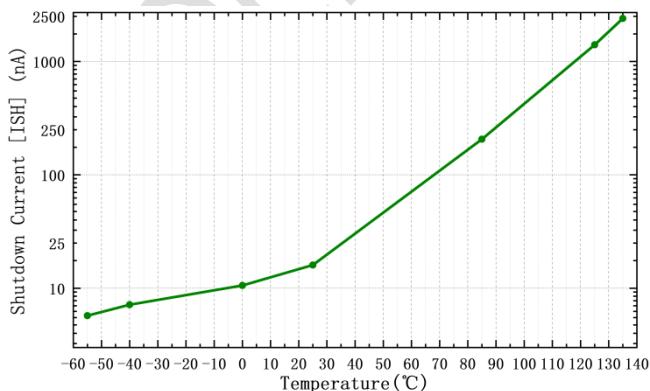


Figure 8. Shutdown Current (ISH) vs. Temperature

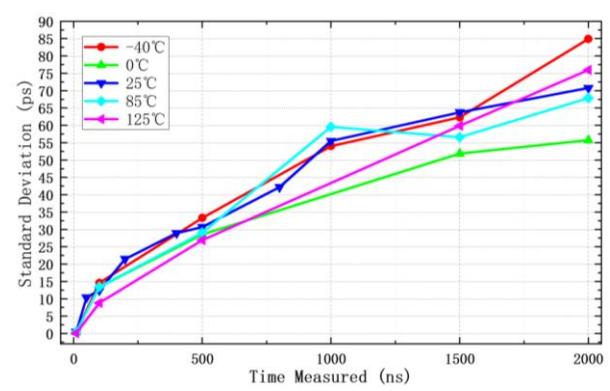


Figure 9. STDEV vs. Temperature & TOF (Measurement Mode 1)

15. Typical Characteristics

VDD = 3.3 V, GND = 0 V, CLOCK = 8 MHz, CALIBRATION2_PERIODS = 10, AVG_CYCLES = 1, one STOP signal.

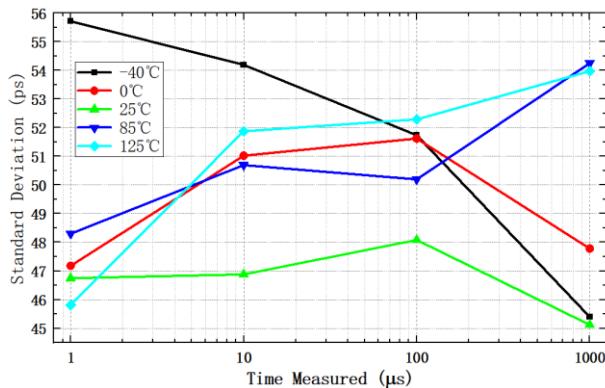


Figure 10. STDEV vs. Temperature & TOF (Measurement Mode 2)

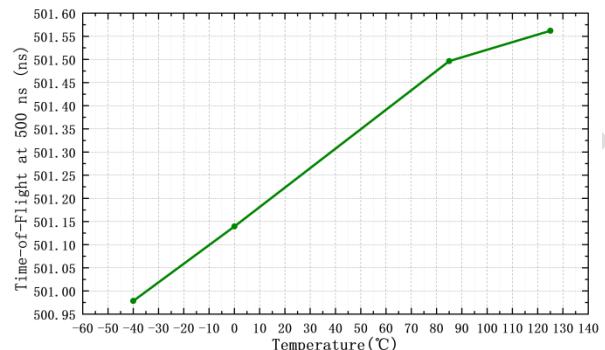


Figure 11. TOF vs. Temperature (Measurement Mode 1)

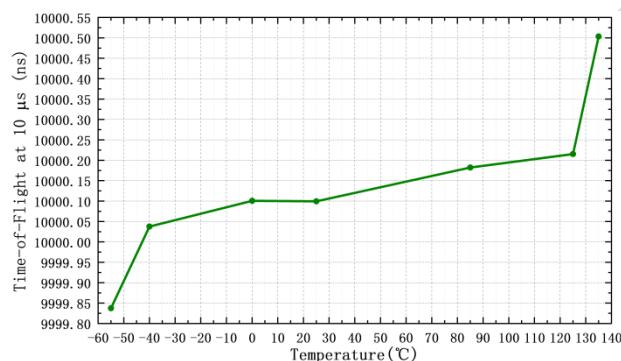


Figure 12. TOF vs. Temperature (Measurement Mode 2)

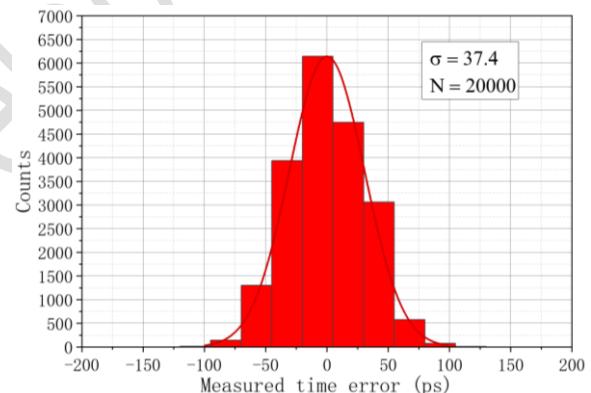


Figure 13. TOF Error Histogram (Measurement Mode 1, 500ns)

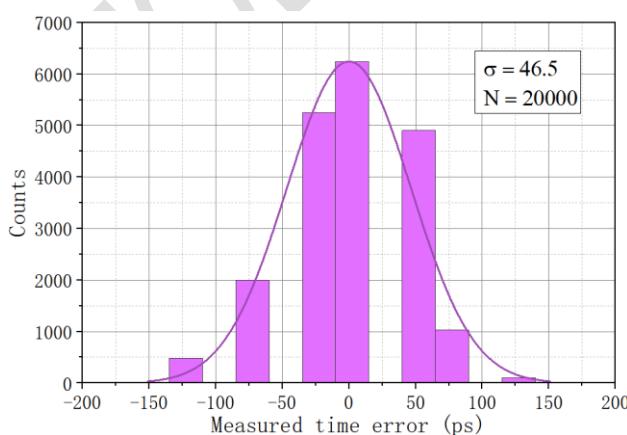


Figure 13. TOF Error Histogram (Measurement Mode 2, 10μs)

16.Register Array

Register Address	Register Name	Description	Bits	Reset Value
00h	CONFIG1	Configuration Register1	8	00h
01h	CONFIG2	Configuration Register2	8	40h
02h	INT_STATUS	Interrupt Status Register	8	00h
03h	INT_MASK	Interrupt Mask Register	8	07h
04h	COARSE_CNTR_OVF_H	Coarse Counter Overflow Value High	8	00h
05h	COARSE_CNTR_OVF_L	Coarse Counter Overflow Value Low	8	FFh
06h	CLOCK_CNTR_OVF_H	CLOCK Counter Overflow Value High	8	FFh
07h	CLOCK_CNTR_OVF_L	CLOCK Counter Overflow Value Low	8	FFh
08h	CLOCK_CNTR_STOP_MASK_H	CLOCK Counter STOP Mask High	8	00h
09h	CLOCK_CNTR_STOP_MASK_L	CLOCK Counter STOP Mask Low	8	00h
10h	TIME1	Measure Time 1	24	00_0000h
11h	CLOCK_COUNT1	CLOCK Counter Value	24	00_0000h
12h	TIME2	Measure Time 2	24	00_0000h
13h	CLOCK_COUNT2	CLOCK Counter Value	24	00_0000h
14h	TIME3	Measure Time 3	24	00_0000h
15h	CLOCK_COUNT3	CLOCK Counter Value	24	00_0000h
16h	TIME 4	Measure Time 4	24	00_0000h
17h	CLOCK_COUNT4	CLOCK Counter Value	24	00_0000h
18h	TIME 5	Measure Time 5	24	00_0000h
19h	CLOCK_COUNT5	CLOCK Counter Value	24	00_0000h
1Ah	TIME6	Measure Time 6	24	00_0000h
1Bh	CALIBRATION1	Calibration 1, 1 CLOCK Period	24	00_0000h
1Ch	CALIBRATION2	Calibration 2, 2/10/20/40 CLOCK Periods	24	00_0000h

Registers of TDC1 or TDC2 are selected for read/write access when their corresponding dedicated SSB1 or SSB2 pin is asserted.

Table 1. Register Summery

TDCx_CONFIG2: Configuration Register 2. R/W (address=00h, SSBx asserted) [reset=0h]**Table 2. TDCx_Configuration Register 1**

7	6	5	4	3	2	1	0
FORCE_CAL	PARITY_EN	TRIGG_EDGE	STOP_EDGE	START_EDGE	MEAS_MODE		START_MEAS
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

R/W=Read/Write; R=Read Only; -n=value after reset

Table 3. TDCx_Configuration Register 1

Bit	Field	Type	Reset	Description
7	FORCE_CAL	R/W	0	0: Calibration is not performed after interrupted measurement (for example, due to counter overflow or missing STOP signal) 1: Calibration is always performed at the end (for example, after a counter overflow)
6	PARITY_EN	R/W	0	0: Parity bit for Measurement Result Registers* disabled (Parity Bit always 0) 1: Parity bit for Measurement Result Registers enabled (Even Parity) *The Measurement Results registers are the TIME1 to TIME6, CLOCK_COUNT1 to CLOCK_COUNT5, CALIBRATION1, CALIBRATION2 registers.
5	TRIGG_EDGE	R/W	0	0: TRIGG is output as a Rising edge signal 1: TRIGG is output as a Falling edge signal
4	STOP_EDGE	R/W	0	0: Measurement is stopped on Rising edge of STOP signal 1: Measurement is stopped on Falling edge of STOP signal
3	START_EDGE	R/W	0	0: Measurement is started on Rising edge of START signal 1: Measurement is started on Falling edge of START signal
[2:1]	MEAS_MODE	R/W	00h	00: Measurement Mode 1 (for expected time-of-flight < 2μs). 01: Measurement Mode 2 (recommended, for expected time-of-flight < 8ms) 10: Measurement Mode 3 (internal 20ns delay and support time of flight 0ns) 11: Measurement Mode 4 (support maximum 1s time-of-flight, but the inner auto average mode measurement times is limited)
0	START_MEAS	R/W	0	Start New Measurement: This bit is cleared when Measurement is Completed. 0: No effect 1: Start New Measurement. Writing a 1 will clear all bits in the Interrupt Status Register and Start the measurement (by generating an TRIGG signal) and will reset the content of all Measurement Results registers.

TDCx_CONFIG2: Configuration Register 2. R/W (address=01h, SSBx asserted) [reset=40h]
Table 4. TDCx_Configuration Register 2

7	6	5	4	3	2	1	0
CALIBRATION2_PERIODS	AVG_CYCLES					NUM_STOP	
R/W-0h	R/W-1h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

R/W=Read/Write; R=Read Only; -n=value after reset

Table 5. TDCx_Configuration Register 2

Bit	Field	Type	Reset	Description
[7:6]	CALIBRATION2_PERIODS	R/W	01h	00: Calibration 2 - measuring 2 CLOCK periods ODS 01: Calibration 2 - measuring 10 CLOCK periods 10: Calibration 2 - measuring 20 CLOCK periods 11: Calibration 2 - measuring 40 CLOCK periods
[5:3]	AVG_CYCLES	R/W	00h	Internal multi-cycle averaging mode. The interrupt is send after a series of measurements is finished. 000: 1 Measurement Cycle only 001: 2 Measurement Cycles 010: 4 Measurement Cycles 011: 8 Measurement Cycles 100: 16 Measurement Cycles 101: 32 Measurement Cycles 110: 64 Measurement Cycles 111: 128 Measurement Cycles
[2:0]	NUM_STOP	R/W	00h	000: Single Stop 001: Two Stops 010: Three Stops 011: Four Stops 100: Five Stops 101, 110, 111: No Effect. Single Stop

TDCx_INT_STATUS: Interrupt Status Register. R/W (address=02h, SSBx asserted) [reset=00h]
Table 6. TDCx_Interrupt Status Register

7	6	5	4	3	2	1	0
Reserved	Reserved	Reserved	MEAS_COMP _FLAG	MEAS_STARTED _FLAG	CLK_CNTR _OVF_INT	COARSE_CNTR _OVF_INT	NEW_MEAS _INT
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

R/W=Read/Write; R=Read Only; -n=value after reset

Table 7. TDCx_Interrupt Status Register Field Description

Bit	Field	Type	Reset	Description
7	Reserved	R/W	0	
6	Reserved	R/W	0	
5	Reserved	R/W	0	
4	MEAS_COMP _FLAG	R/W	0	Writing a 1 will clear the status 0: Measurement has not completed 1: Measurement has completed
3	MEAS_STARTED _FLAG	R/W	0	Writing a 1 will clear the status 0: Measurement has not started 1: Measurement has started (START signal received)
2	CLK_CNTR _OVF_INT	R/W	0	Requires writing a 1 to clear interrupt status 0: No overflow detected 1: Clock overflow detected, running measurement will be stopped immediately
1	COARSE_CNTR _OVF_INT	R/W	0	Requires writing a 1 to clear interrupt status 0: No overflow detected 1: Coarse overflow detected, running measurement will be stopped immediately
0	NEW_MEAS _INT	R/W	0	Requires writing a 1 to clear interrupt status 0: Interrupt not detected 1: Interrupt detected – New Measurement has been completed

TDCx_INT_MASK: Interrupt Mask Register. R/W (address=03h, SSBx asserted) [reset=07h]
Table 8. TDCx_Interrupt Mask Register

7	6	5	4	3	2	1	0
Reserved	Reserved	Reserved	Reserved	Reserved	CLOCK_CNTR_OVF_MASK	COARSE_CNTR_OVF_MASK	NEW_MEAS_MASK
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-1h	R/W-1h	R/W-1h

R/W=Read/Write; R=Read Only; -n=value after reset

Table 9. TDCx_Interrupt Mask Register Field Description

Bit	Field	Type	Reset	Description
7	Reserved	R/W	0	
6	Reserved	R/W	0	
5	Reserved	R/W	0	
4	Reserved	R/W	0	
3	Reserved	R/W	0	
2	CLOCK_CNTR_OVF_MASK	R/W	1	0: CLOCK Counter Overflow Interrupt disabled 1: CLOCK Counter Overflow Interrupt enabled
1	COARSE_CNTR_OVF_MASK	R/W	1	0: Coarse Counter Overflow Interrupt disabled 1: Coarse Counter Overflow Interrupt enabled
0	NEW_MEAS_MASK	R/W	1	0: New Measurement Interrupt disabled 1: New Measurement Interrupt enabled

TDCx_COARSE_CNTR_OVF_H: Coarse Counter Overflow High Value Register (address = 04h, SSBx asserted) [reset=FFh]

Table 10. TDCx_Coarse Counter Overflow High Value Register

7	6	5	4	3	2	1	0
COARSE_CNTR_OVF_H							
R/W-1h	R/W-1h	R/W-1h	R/W-1h	R/W-1h	R/W-1h	R/W-1h	R/W-1h

R/W=Read/Write; R=Read Only; -n=value after reset

Table 11. TDCx_Coarse Counter Overflow High Value Register Field Description

Bit	Field	Type	Reset	Description			
7:0	COARSE_CNTR_OVF_H	R/W	FFh	Coarse Counter Overflow Value, higher 8 Bit			

TDCx_COARSE_CNTR_OVF_L: Coarse Counter Overflow Low Value Register (address = 05h, SSBx asserted) [reset=FFh]

Table 12. TDCx_Coarse Counter Overflow Low Value Register

7	6	5	4	3	2	1	0
COARSE_CNTR_OVF_L							
R/W-1h	R/W-1h	R/W-1h	R/W-1h	R/W-1h	R/W-1h	R/W-1h	R/W-1h

R/W=Read/Write; R=Read Only; -n=value after reset

Table 13. TDCx_Coarse Counter Overflow Low Value Register Field Description

Bit	Field	Type	Reset	Description			
7:0	COARSE_CNTR_OVF_L	R/W	FFh	Coarse Counter Overflow Value, lower 8 Bit Note: Don't set COARSE_CNTR_OVF_L to 1.			

TDCx_CLOCK_CNTR_OVF_H: Clock Counter Overflow High Register (address = 06h, SSBx asserted)
[reset = FFh]

Table 14. TDCx_Clock Counter Overflow High Register

7	6	5	4	3	2	1	0
CLOCK_CNTR_OVF_H							
R/W-1h	R/W-1h	R/W-1h	R/W-1h	R/W-1h	R/W-1h	R/W-1h	R/W-1h

R/W=Read/Write; R=Read Only; -n=value after reset

Table 15. TDCx_Clock Counter Overflow High Register Field Description

Bit	Field	Type	Reset	Description
7:0	CLOCK_CNTR_OVF_H	R/W	FFh	CLOCK Counter Overflow Value, upper 8 Bit

TDCx_CLOCK_CNTR_OVF_L: Clock Counter Overflow High Register (address = 07h, SSBx asserted)
[reset = FFh]

Table 16. TDCx_Clock Counter Overflow High Register

7	6	5	4	3	2	1	0
CLOCK_CNTR_OVF_L							
R/W-1h	R/W-1h	R/W-1h	R/W-1h	R/W-1h	R/W-1h	R/W-1h	R/W-1h

R/W=Read/Write; R=Read Only; -n=value after reset

Table 17. TDCx_Clock Counter Overflow High Register Field Description

Bit	Field	Type	Reset	Description
7:0	CLOCK_CNTR_OVF_L	R/W	FFh	CLOCK Counter Overflow Value, lower 8 Bit

TDCx_CLOCK_CNTR_STOP_MASK_H: CLOCK Counter STOP Mask High Value Register (address = 08h, SSBx asserted) [reset = 00h]

Table 18. TDCx_CLOCK Counter STOP Mask High Value Register

7	6	5	4	3	2	1	0
CLOCK_CNTR_STOP_MASK_H							
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

R/W=Read/Write; R=Read Only; -n=value after reset

Table 19. CLOCK Counter STOP Mask High Value Register Field Description

Bit	Field	Type	Reset	Description			
7:0	CLOCK_CNTR_STOP_MASK_H	R/W	00h	CLOCK Counter STOP Mask, upper 8 Bit			

TDCx_CLOCK_CNTR_STOP_MASK_L: CLOCK Counter STOP Mask Low Value Register (address = 09h, SSBx asserted) [reset = 00h]

Table 20. TDCx_CLOCK Counter STOP Mask Low Value Register

7	6	5	4	3	2	1	0
CLOCK_CNTR_STOP_MASK_L							
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

R/W=Read/Write; R=Read Only; -n=value after reset

Table 21. TDCx_CLOCK Counter STOP Mask Low Value Register Field Description

Bit	Field	Type	Reset	Description			
7:0	CLOCK_CNTR_STOP_MASK_L	R/W	00h	CLOCK Counter STOP Mask, lower 8 Bit			

TDCx_TIME1: Time 1 Register (address: 10h, SSBx asserted) [reset = 00_0000h]
Table 22. TDCx_TIME1 Register

23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Parity Bit	Measurement Result: 23 bit integer value (Bit 22: MSB, Bit 0: LSB)																						
R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0

R/W=Read/Write; R=Read Only; -n=value after reset

Table 23. TDCx_TIME1 Register Field Descriptions

Bit	Field	Type	Reset	Description
23	Parity Bit	R	0	Parity Bit
22-0	Measurement Result: 23 bit integer value (Bit 22: MSB, Bit 0: LSB)	R	0	Measurement Result

TDCx_CLOCK_COUNT1: Clock Count Register (address: 11h, SSBx asserted) [reset = 00_0000h]
Table 24. TDCx_CLOCK_COUNT1

23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Parity Bit	CLOCK_COUNT1 Result																						
R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0

R/W=Read/Write; R=Read Only; -n=value after reset

Table 25. TDCx_CLOCK_COUNT1 Field Description

Bit	Field	Type	Reset	Description
23	Parity Bit	R	0	Parity Bit
22-16	Not Used	R	0	Measurement Result
15-0	CLOCK_COUNT1 Measurement Result	R	0	CLOCK_COUNT1 Measurement Result

TDCx_TIME2: Time 2 Register (address: 12h, SSBx asserted) [reset = 00_0000h]**Table 26. TDCx_TIME 2 Register**

23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Parity Bit	Measurement Result: 23 bit integer value (Bit 22: MSB, Bit 0: LSB)																						
R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0

R/W=Read/Write; R=Read Only; -n=value after reset

Table 27. TDCx_TIME 2 Register Field Descriptions

Bit	Field	Type	Reset	Description
23	Parity Bit	R	0	Parity Bit
22-0	Measurement Result: 23 bit integer value (Bit 22: MSB, Bit 0: LSB)	R	0	Measurement Result

TDCx_CLOCK_COUNT2: Clock Count Register (address: 13h, SSBx asserted) [reset = 00_0000h]**Table 28. TDCx_CLOCK_COUNT2**

23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Parity Bit	CLOCK_COUNT2 Result																						
R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0

R/W=Read/Write; R=Read Only; -n=value after reset

Table 29. TDCx_CLOCK_COUNT2 Field Description

Bit	Field	Type	Reset	Description
23	Parity Bit	R	0	Parity Bit
22-16	Not Used	R	0	Measurement Result
15-0	CLOCK_COUNT2 Measurement Result	R	0	CLOCK_COUNT2 Measurement Result

TDCx_TIME3: Time 3 Register (address: 14h, SSBx asserted) [reset = 00_0000h]
Table 30. TDCx_TIME 3 Register

23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Parity Bit	Measurement Result: 23 bit integer value (Bit 22: MSB, Bit 0: LSB)																						
R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0

R/W=Read/Write; R=Read Only; -n=value after reset

Table 31. TDCx_TIME 3 Register Field Descriptions

Bit	Field	Type	Reset	Description
23	Parity Bit	R	0	Parity Bit
22-0	Measurement Result: 23 bit integer value (Bit 22: MSB, Bit 0: LSB)	R	0	Measurement Result

TDCx_CLOCK_COUNT3: Clock Count Register (address: 15h, SSBx asserted) [reset = 00_0000h]
Table 32. TDCx_CLOCK_COUNT3

23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Parity Bit	CLOCK_COUNT3 Result																						
R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0

R/W=Read/Write; R=Read Only; -n=value after reset

Table 33. TDCx_CLOCK_COUNT3 Field Description

Bit	Field	Type	Reset	Description
23	Parity Bit	R	0	Parity Bit
22-16	Not Used	R	0	Measurement Result
15-0	CLOCK_COUNT3 Measurement Result	R	0	CLOCK_COUNT3 Measurement Result

TDCx_TIME4: Time 4 Register (address: 16h, SSBx asserted) [reset = 00_0000h]**Table 34. TDCx_TIME 4 Register**

23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Parity Bit	Measurement Result: 23 bit integer value (Bit 22: MSB, Bit 0: LSB)																						
R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0

R/W=Read/Write; R=Read Only; -n=value after reset

Table 35. TDCx_TIME 4 Register Field Descriptions

Bit	Field	Type	Reset	Description
23	Parity Bit	R	0	Parity Bit
22-0	Measurement Result: 23 bit integer value (Bit 22: MSB, Bit 0: LSB)	R	0	Measurement Result

TDCx_CLOCK_COUNT4: Clock Count Register (address: 17h, SSBx asserted) [reset = 00_0000h]**Table 36. TDCx_CLOCK_COUNT4**

23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Parity Bit	CLOCK_COUNT4 Result																						
R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0

R/W=Read/Write; R=Read Only; -n=value after reset

Table 37. TDCx_CLOCK_COUNT4 Field Description

Bit	Field	Type	Reset	Description
23	Parity Bit	R	0	Parity Bit
22-16	Not Used	R	0	Measurement Result
15-0	CLOCK_COUNT4 Measurement Result	R	0	CLOCK_COUNT4 Measurement Result

TDCx_TIME5: Time 5 Register (address: 18h, SSBx asserted) [reset = 00_0000h]
Table 38. TDCx_TIME 5 Register

23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Parity Bit	Measurement Result: 23 bit integer value (Bit 22: MSB, Bit 0: LSB)																						
R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0

R/W=Read/Write; R=Read Only; -n=value after reset

Table 39. TDCx_TIME 5 Register Field Descriptions

Bit	Field	Type	Reset	Description
23	Parity Bit	R	0	Parity Bit
22-0	Measurement Result: 23 bit integer value (Bit 22: MSB, Bit 0: LSB)	R	0	Measurement Result

TDCx_CLOCK_COUNT5: Clock Count Register (address: 19h, SSBx asserted) [reset = 00_0000h]
Table 40. TDCx_CLOCK_COUNT5

23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Parity Bit	CLOCK_COUNT5 Result																						
R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0

R/W=Read/Write; R=Read Only; -n=value after reset

Table 41. TDCx_CLOCK_COUNT5 Field Description

Bit	Field	Type	Reset	Description
23	Parity Bit	R	0	Parity Bit
22-16	Not Used	R	0	Measurement Result
15-0	CLOCK_COUNT5 Measurement Result	R	0	CLOCK_COUNT5 Measurement Result

TDCx_TIME6: Time 6 Register (address: 1Ah, SSBx asserted) [reset = 00_0000h]**Table 42. TDCx_TIME 6 Register**

23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Parity Bit	Measurement Result: 23 bit integer value (Bit 22: MSB, Bit 0: LSB)																						
R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0

R/W=Read/Write; R=Read Only; -n=value after reset

Table 43. TDCx_TIME 6 Register Field Descriptions

Bit	Field	Type	Reset	Description
23	Parity Bit	R	0	Parity Bit
22-0	Measurement Result: 23 bit integer value (Bit 22: MSB, Bit 0: LSB)	R	0	Measurement Result

TDCx_CALIBRATION1: Calibration 1 Register (address: 1Bh, SSBx asserted) [reset = 00_0000h]**Table 44. TDCx_CALIBRATION1 Register**

23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Parity Bit	Calibration 1																						
R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0

R/W=Read/Write; R=Read Only; -n=value after reset

Table 45. TDCx_CALIBRATION1 Field Description

Bit	Field	Type	Reset	Description
23	Parity Bit	R	0	Parity Bit
22-0	Calibration1	R	0	Calibration 1 Result: 23 bit integer value (Bit 22: MSB, Bit 0: LSB)

TDCx_CALIBRATION2: Calibration 2 Register (address: 1Ch, SSBx asserted) [reset = 00_0000h]**Table 46. TDCx_CALIBRATION2 Register**

23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Parity Bit	Calibration 2																						
R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0

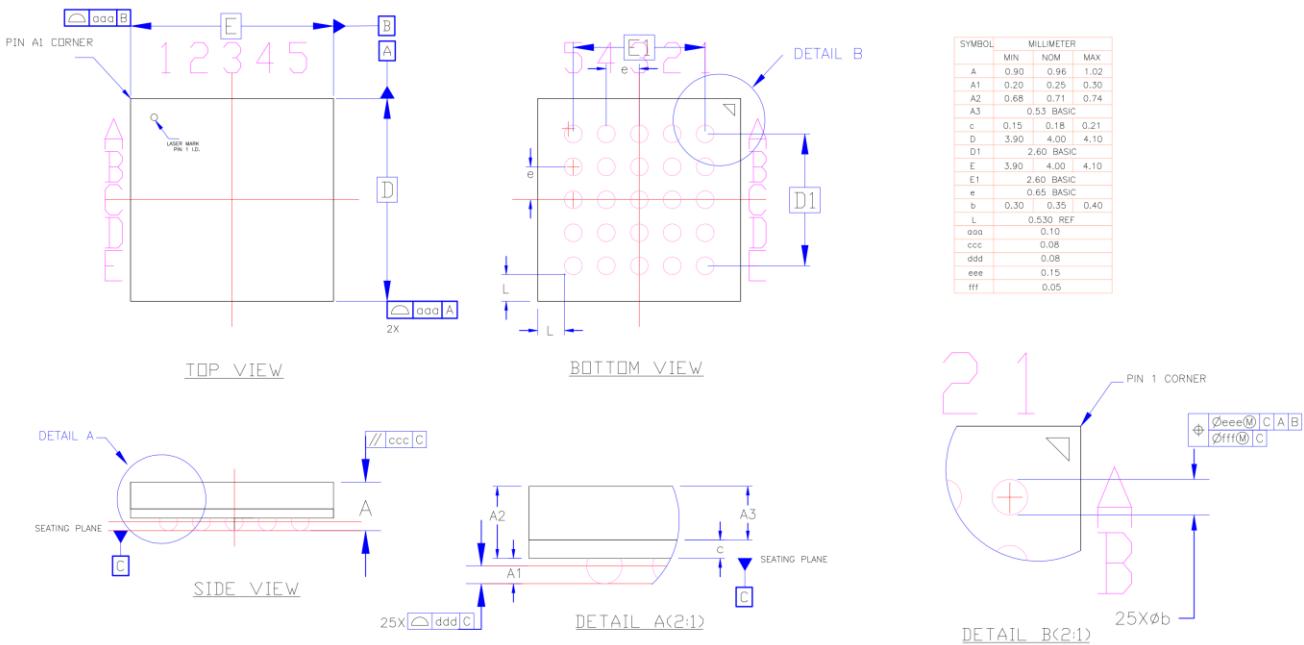
R/W=Read/Write; R=Read Only; -n=value after reset

Table 47. CALIBRATION2 Register Field Description

Bit	Field	Type	Reset	Description
23	Parity Bit	R	0	Parity Bit
22-0	Calibration1	R	0	Calibration 2 Result: 23 bit integer value (Bit 22: MSB, Bit 0: LSB)

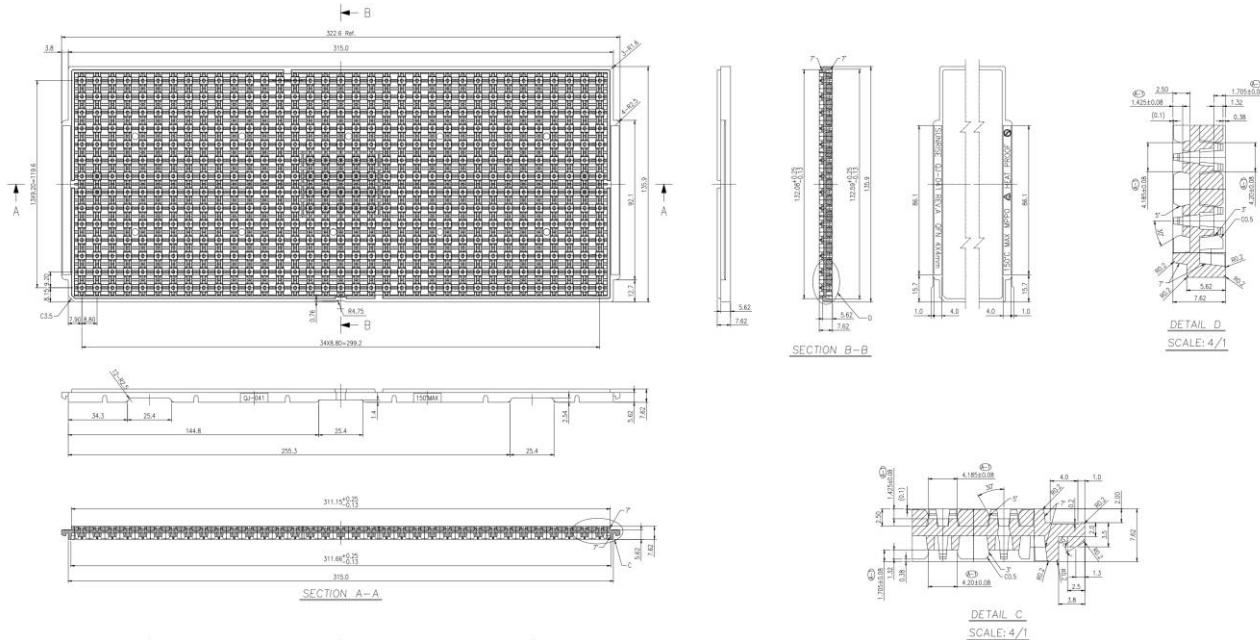
17. PACKAGE INFORMATION

FBGA4x4-25



18. TRAY INFORMATION

FBGA 4mmx4mm JEDEC Tray



Note:

- 1) All Dimensions are in Millimeter
- 2) Quantity of Units per Tray is 490
- 3) MSL level is level 3.

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