FEATURES

- LIN 2.x/ISO 17987-4:2016 (12V)/SAE J2602 compliant
- Thermally protected
- Transmit data (TXD) dominant time-out function
- Bus terminal current limit protected
- Under voltage on battery
- Very low current consumption in Sleep mode
- Support local and remote wake-up
- Enable an external high voltage regulator by INH
- Baud rates up to 20 kBd
- Very low ElectroMagnetic Emission (EME)
- High ElectroMagnetic Immunity (EMI)
- Available in SO8 and DFN3*3-8 packages

PRODUCT APPEARANCE

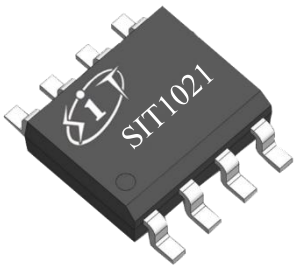


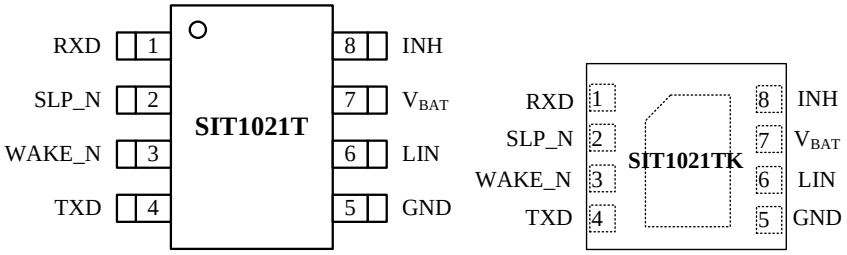
Fig 1. Provide green and environmentally friendly lead-free package

DESCRIPTION

The SIT1021 is a physical layer transceiver of Local Interconnect Network (LIN). It is compliant with LIN 2.0/LIN 2.1/LIN 2.2/LIN 2.2A/ISO 17987-4:2016 (12V) and SAE J2602 standards. It is typically used for low speed in-vehicle networks using baud rates from 1 kBd to 20 kBd. The LIN protocol data stream at the transmit data input (TXD) is converted by the SIT1021 into a bus signal with optimized wave shaping to minimize ElectroMagnetic Emission (EME). The SIT1021 converts the data stream on LIN bus to logic level signals that are sent to the microprocessor via the pin RXD. The LIN bus is pulled high by the internal slave resistor and a series diode. Master applications require an external pull-up resistor in series with a diode to connect pin VBAT and pin LIN.

The SIT1021 has an extremely low current consumption in sleep mode. The power consumption is reduced to a minimum if in failure modes. It also provides a high voltage output pin INH to enable an external high voltage regulator which used to support the microprocessor.

PIN CONFIGURATION



(a) SOP8 package (b) DFN3*3-8 package

Fig 2. SIT1021 pin configuration diagrams

PIN DESCRIPTION

Table 1. Pin description

Pin	Symbol	Description
1	RXD	receive data output (open-drain); active LOW after a wake-up event.
2	SLP_N	sleep control input (active LOW); controls inhibit output; resets wake-up source flag on TXD and wake-up request on RXD.
3	WAKE_N	local wake-up input (active LOW); negative edge triggered.
4	TXD	transmit data input; active LOW output after a local wake-up event.
5	GND	Ground.
6	LIN	LIN bus line input/output.
7	V_{BAT}	battery supply voltage.
8	INH	battery related inhibit output for controlling an external voltage regulator; active HIGH after a wake-up event.

NOTE: The exposed center pad of the DFN3*3-8 package is internal connected to the GND PIN of the Chip. For enhanced thermal performance, the exposed center pad of the DFN3*3-8 package could be soldered to board ground.

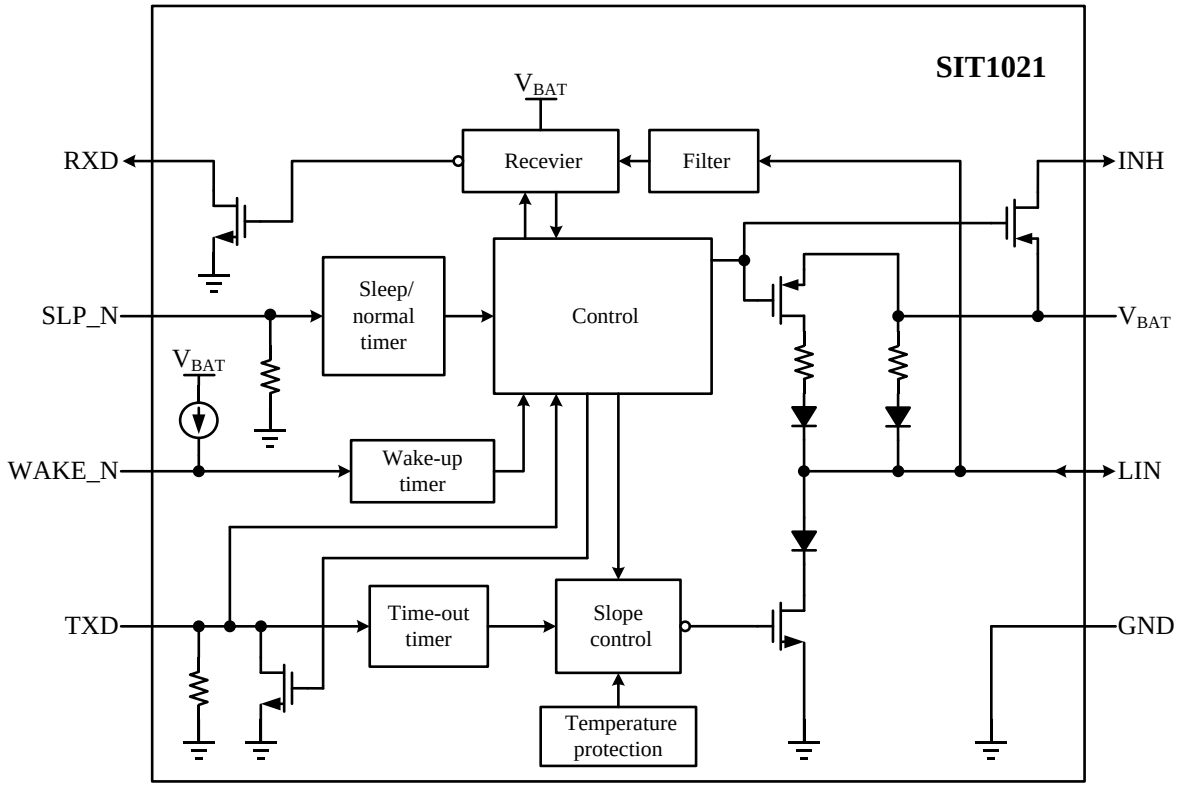


Fig 3. Block diagram

FEATURE DESCRIPTION

1 Overview

The SIT1021 is an interface device used between the LIN protocol controller and the physical bus. It can be used for in-vehicle and industrial control with a data rate up to 20kBd. The SIT1021 receives the data stream sent by protocol controller at the pin TXD, and converts it into a bus signal with appropriate slew rate and waveform shaping. The input data on LIN bus is output to external microcontroller by pin RXD. This device is compliant with LIN 2.0/LIN 2.1/LIN 2.2/LIN 2.2A/ISO 17987-4:2016 (12V) and SAE J2602 standards.

2 Short-circuit protection

Pin TXD provides an internal pull-down to GND to apply a predefined level on TXD when it is not enabled. The pin SLP_N also provides an internal pull-down to force the transceiver to enter sleep mode when SLP_N is not enabled.

Pin RXD will be left floating and limit the output current of transmitter to prevent a short-circuit between LIN and VBAT or GND if the supply on pin VBAT is turned off. There is no reverse current at the bus terminal, and the connection between LIN supply can be shut off without affecting the bus.

3 Thermal Shutdown

In normal mode, the over-temperature protection circuit will disable the output driver when the junction temperature of SIT1021 exceeds the shutdown junction temperature $T_{j(sd)}$. The driver is enabled again when the junction temperature has dropped below $T_{j(sd)}$ and a recessive level is present at pin TXD.

4 TXD dominant time-out function

A TXD dominant time-out timer circuit prevents the bus lines from being driven to a permanent dominant state (blocking all network communication) if pin TXD is forced permanently LOW by a hardware and/or software application failure. The timer is triggered by a negative edge on pin TXD. If the duration of the LOW level on pin TXD exceeds the internal timer value (t_{dom}), the transmitter is disabled, driving the bus lines into a recessive state. The timer is reset by a positive edge on pin TXD.

5 Operating modes

As shown in Fig 4, the SIT1021 supports four functional modes for normal operation (Normal mode), power-up (Power-on mode), standby operation (Standby mode) and very-low-power operation (Sleep mode). The operating states in each mode are shown in Table 2.

Sleep mode: This mode is the most power saving mode of the SIT1021. It can be woken up remotely via pin LIN, or woken up locally via pin WAKE_N, or activated directly via pin SLP_N. The pin WAKE_N, pin SLP_N and pin LIN are filtered to prevent accidental wake up events. The wake-up events for SIT1021 in sleep mode is: the remote wake up time via pin LIN must be longer than $t_{wake(dom)LIN}$; the local wake up time via pin WAKE_N must be longer than $t_{wake(dom)WAKE\_N}$; the time wake up directly via pin SLP_N must be

longer than $t_{gotonorm}$.

Sleep mode is only entered when the pin SLP_N is low and from normal mode. To enter Sleep mode successfully (INH becomes floating), the sleep command (SLP_N = 0) must be maintained for at least $t_{gotosleep}$. The pin INH is only floating in sleep mode and going into high in others modes.

Standby mode: It is entered whenever a local or remote wake-up occurs while the device is in Sleep mode. Standby mode is signaled through a low level on pin RXD. The pin INH will be set high and activate the external voltage regulator and the microcontroller after the device enters standby mode from sleep mode.

Setting pin SLP_N high during Standby mode results in the following events:

(1) An immediate reset of the wake-up source flag; thus, releasing the possible strong pull-down at pin TXD before the actual mode change (after $t_{gotonorm}$) is performed.

(2) A change into Normal mode if the high level on pin SLP_N has been maintained for a certain time period ($t_{gotonorm}$).

(3) An immediate reset of the wake-up request signal on pin RXD.

Normal mode: Only in Normal mode the receiver and transmitter are active and the SIT1021 is able to transmit and receive data via the LIN bus. The high level of bus represents recessive and low level represents dominant. The receiver detects the data stream on the LIN bus and outputs it to the microcontroller via pin RXD. Normal mode is entered as a high level on pin SLP_N and maintained for a time of at least $t_{gotonorm}$ while the SIT1021 is in Sleep, Power-up or Standby mode. The Sleep mode is entered by setting pin SLP_N low for longer than $t_{gotosleep}$.

Power-on mode: When SIT1021 is in Power-on mode: pin RXD is left floating, pin TXD is weakly pulled down, transmitter and receiver are not activated. If the pin SLP_N is high at power up the device will power up in normal mode and if low will power up in standby mode.

6 Wake-up source recognition

In Sleep mode, SIT1021 can wake up remotely via the LIN bus or wake up locally via the pin WAKE_N. The wake-up source flag can be read by detecting the state of pin TXD in the Standby mode. If an external pull-up resistor on pin TXD to the power supply voltage of the microcontroller has been added, a high level indicates a remote wake-up request (weak pull-down at pin TXD) and a LOW level indicates a local wake-up request (strong pull-down at pin TXD; much stronger than the external pull-up resistor). The wake-up request flag (signaled on pin RXD) as well as the wake-up source flag (signaled on pin TXD) are reset immediately after the microcontroller sets pin SLP_N high.

7 Wake Up Events

In sleep mode, the device can be woken up by the following three ways:

(1) Remote wake-up via pin LIN;

(2) Local wake-up via pin WAKE_N;

(3) Wake up directly via pin SLP_N.

8 Remote and local wake-up

Remote wake-up on the pin LIN: When A falling edge at pin LIN followed by a low level maintained longer than $t_{wake(dom)LIN}$ and a rising edge at pin LIN respectively, the process is regarded as a valid remote wake-up event (see Fig 5).

Local wake-up on the pin WAKE_N: When A falling edge at pin LIN followed by a low level maintained longer than $t_{wake(dom)WAKE\_N}$, the process is regarded as a valid remote wake-up event. The pin WAKE_N provides an internal pull-up path to VBAT. To prevent EMI issues, it is recommended to connect the unused pin WAKE_N to VBAT.

When a local or remote wake-up occurs, pin INH is activated (turns to high) and the internal slave termination resistor is turned on. The wake-up request is indicated by a low active wake-up request signal on pin RXD to interrupt the microcontroller.

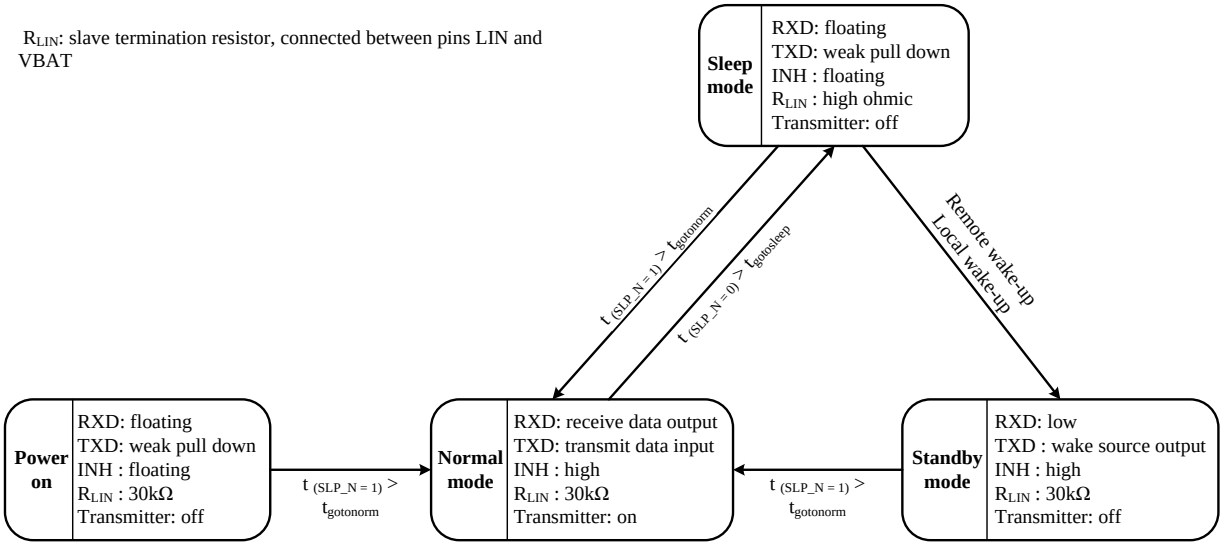


Fig 4. State diagram

Table 2. Operating modes

Mode	SLP_N	TXD	RXD	INH	Transmitter	Remarks
Sleep	low	weak pull-down	floating	floating	off	no wake-up request detected
Standby	low	weak pull-down if remote wake-up; strong pull-down if local wake-up	low	high	off	wake-up request detected; in this mode the microcontroller can read the wake-up source: remote or local wake-up
Normal	high	recessive: high dominant: low	recessive: high dominant: low	high	on	
Power-on	low	weak pull-down	floating	high	off	

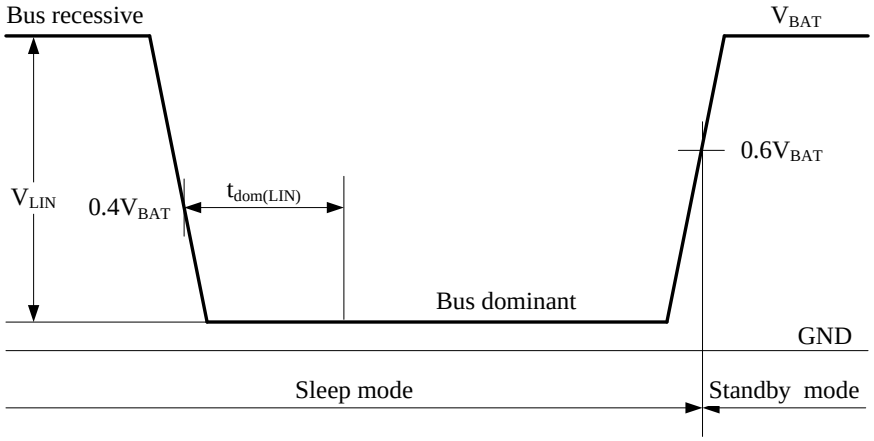


Fig 5. Remote wake-up behavior

LIMITING VALUES

Parameter	Symbol	Conditions	Range	Unit
battery supply voltage	V_{BAT}	with respect to GND	-0.3 ~ +42	V
voltage on pin TXD	V_{TXD}	I_{SLP_N} no limitation	-0.3 ~ +6	V
		I_{SLP_N} < 500μA	-0.3 ~ +7	
voltage on pin RXD	V_{RXD}	I_{SLP_N} no limitation	-0.3 ~ +6	V
		I_{SLP_N} < 500μA	-0.3 ~ +7	
voltage on pin SLP_N	V_{SLP_N}	I_{SLP_N} no limitation	-0.3 ~ +6	V
		I_{SLP_N} < 500μA	-0.3 ~ +7	
voltage on pin LIN	V_{LIN}	with respect to GND	-42 ~ +42	V
voltage on pin WAKE_N	V_{WAKE_N}		-0.3 ~ +42	V
voltage on pin INH	V_{INH}		-0.3 ~ V_{BAT}+0.3	V
virtual junction temperature	T_j		-40 ~ 150	°C
storage temperature	T_{stg}		-55 ~ 150	°C

The maximum limit parameters mean that exceeding these values may cause irreversible damage to the device. Under these conditions, it is not conducive to the normal operation of the device. The continuous operation of the device at the maximum allowable rating may affect the reliability of the device. The reference point for all voltages is ground.

STATIC CHARACTERISTICS

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Supply						
battery supply current	I_{BAT}	Sleep mode; (V_{LIN}=V_{BAT}; V_{WAKE_N}=V_{BAT}; V_{TXD}=0V; V_{SLP_N}=0V)	1	3	15	μA
		Standby mode; bus recessive (V_{INH}=V_{BAT}; V_{LIN}=V_{BAT}; V_{WAKE_N}=V_{BAT}; V_{TXD}=0V; V_{SLP_N}=0V)	150	350	800	μA
		Standby mode; bus dominant (V_{BAT}=12V; V_{INH}=12V; V_{LIN}=0V; V_{WAKE_N}=12V; V_{TXD}=0V; V_{SLP_N}=0V)	500	750	1000	μA
		Normal mode; bus recessive (V_{INH}=V_{BAT}; V_{LIN}=V_{BAT}; V_{WAKE_N}=V_{BAT}; V_{TXD}=5V; V_{SLP_N}=5V)	200	380	600	μA
		Normal mode; bus dominant (V_{BAT}=12V; V_{INH}=12V; V_{WAKE_N}=12V; V_{TXD}=0V; V_{SLP_N}=5V)	0.5	1.4	3	mA
Power-on reset						
low-level V_{BAT} reset threshold voltage	$V_{th}(V_{BATL})L$		3.9	4.4	4.7	V
high-level V_{BAT} reset threshold voltage	$V_{th}(V_{BATL})H$		4.2	4.7	5.1	V
V_{BAT} reset hysteresis voltage	$V_{hys}(V_{BATL})$		0.05	0.3	1	V

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Pin TXD						
high-level input voltage	V_{IH}		2		7	V
low-level input voltage	V_{IL}		-0.3		+0.8	V
hysteresis voltage	V_{hys}		50	200	400	mV
pull-down resistance on pin TXD	$R_{PD(TXD)}$	V_{TXD}=5V	140	500	1200	kΩ
low-level input current	I_{IL}	V_{TXD}=0V	-5		+5	μA
low-level output current	I_{OL}	local wake-up request; Standby mode; V_{WAKE_N}=0V; V_{LIN}=V_{BAT}; V_{TXD}=0.4V	1.5			mA
Pin SLP_N						
high-level input voltage	V_{IH}		2		7	V
low-level input voltage	V_{IL}		-0.3		0.8	V
hysteresis voltage	V_{hys}		50	200	400	mV
pull-down resistance on pin SLP_N	$R_{PD(SLP\_N)}$	V_{SLP_N}=5V	140	500	1200	kΩ
low-level input current	I_{IL}	V_{SLP_N}=0V	-5		5	μA
Pin RXD						
low-level output current	I_{OL}	Normal mode; V_{RXD}=0.4V; V_{LIN}=0V	1.5			mA
high-level leakage current	I_{LH}	Normal mode; V_{RXD}=5V; V_{LIN}=V_{BAT}	-5		5	μA
Pin WAKE_N						
high-level input voltage	V_{IH}		V_{BAT}-1		V_{BAT} +0.3	V
low-level input voltage	V_{IL}		-0.3		V_{BAT}-3.3	V

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
low-level pull-up current	$I_{pu(L)}$	V_{WAKE_N}=0V;	-30	-12	-1	μA
high-level leakage current	I_{LH}	V_{WAKE_N}=27V; V_{BAT}=27V	-5		5	μA
Pin INH						
switch-on resistance between pins V_{BAT} and INH	R_{SW}	Standby; Normal and Power-on mode; I_{INH}=-15mA; V_{BAT}=12V		20	50	Ω
high-level leakage current	I_{LH}	Sleep mode; V_{INH}=27V; V_{BAT}=27V	-5		5	μA
Pin LIN						
current limitation for driver dominant state	I_{BUS_LIM}	V_{TXD}=0V; V_{LIN}=V_{BAT}=18V	40		100	mA
pull-up resistance	R_{pu}	Sleep mode; V_{SLP_N}=0V	50	160	250	kΩ
receiver recessive input leakage current	$I_{BUS\_PAS\_rec}$	V_{TXD}=5V; V_{LIN}=27V; V_{BAT}=5.5V			10	μA
receiver dominant input leakage current including pull-up resistor	$I_{BUS\_PAS\_dom}$	Normal mode; V_{TXD}=5V; V_{LIN}=0V; V_{BAT}=12V	-1000			μA
loss-of-ground bus current	$I_{BUS\_NO\_GND}$	V_{BAT}=27V; V_{LIN}=0V	-1000		10	μA
loss-of-battery bus current	$I_{BUS\_NO\_BAT}$	V_{BAT}=0V; V_{LIN}=27V			10	μA
receiver dominant input voltage	$V_{th(dom)RX}$				0.4V_{BAT}	V
receiver recessive input voltage	$V_{th(rec)RX}$		0.6V_{BAT}			V
receiver center voltage	$V_{th(RX)cntr}$	$V_{th(RX)\ cntr}$= ($V_{th(rec)RX}$+ $V_{th(dom)RX}$)/2	0.475V_{BAT}	0.5 V_{BAT}	0.525V_{BAT}	V
receiver hysteresis voltage	$V_{th(hys)RX}$	$V_{th(hys)RX}$= $V_{th(rec)RX}$-$V_{th(dom)RX}$			0.175V_{BAT}	V
slave resistance	R_{slave}	connected between pins LIN and V_{BAT}; V_{LIN}=0V; V_{BAT}=12V; V_{TXD}=V_{SLP_N}=5V	20	30	60	kΩ

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
capacitance on pin LIN	C_{LIN}				30	pF
dominant output voltage	$V_{o(dom)}$	Normal mode; V_{TXD}=0V; V_{BAT}=7V			1.4	V
		Normal mode; V_{TXD}=0V; V_{BAT}=18V			2.0	V
Thermal shutdown						
shutdown junction temperature	$T_{j(sd)}$		150	175	200	°C

(Unless specified otherwise; 5.5V≤V_{BAT}≤27V, -40°C≤T_j≤150°C; typical in V_{BAT}=12V, T_j=25°C.)

DYNAMIC CHARACTERISTICS

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Duty cycles						
duty cycle 1	δ1 [1][2]	$V_{th(rec)(max)}$=0.744×V_{BAT}; $V_{th(dom)(max)}$=0.581×V_{BAT}; t_{bit}=50μs; V_{BAT}=7V~18V Fig 6	0.396			
		$V_{th(rec)(max)}$=0.76×V_{BAT}; $V_{th(dom)(max)}$=0.593×V_{BAT}; t_{bit}=50μs; V_{BAT}=5.5V~7V Fig 6	0.396			
duty cycle 2	δ2 [2][3]	$V_{th(rec)(min)}$=0.422×V_{BAT}; $V_{th(dom)(min)}$=0.284×V_{BAT}; t_{bit}=50μs; V_{BAT}=7.6V~18V Fig 6			0.581	
		$V_{th(rec)(min)}$=0.41×V_{BAT}; $V_{th(dom)(min)}$=0.275×V_{BAT}; t_{bit}=50μs; V_{BAT}=6.1V~7.6V Fig 6			0.581	
duty cycle 3	δ3 [1][2]	$V_{th(rec)(max)}$=0.778×V_{BAT}; $V_{th(dom)(max)}$=0.616×V_{BAT}; t_{bit}=96μs; V_{BAT}=7V~18V Fig 6	0.417			
		$V_{th(rec)(max)}$=0.797×V_{BAT}; $V_{th(dom)(max)}$=0.630×V_{BAT}; t_{bit}=96μs; V_{BAT}=5.5V~7V Fig 6	0.417			

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
duty cycle 4	δ4 [2][3]	$V_{th(rec)(min)}$=0.389×V_{BAT}; $V_{th(dom)(min)}$=0.251×V_{BAT}; t_{bit}=96μs; V_{BAT}=7.6V~18V Fig 6			0.590	
		$V_{th(rec)(min)}$=0.378×V_{BAT}; $V_{th(dom)(min)}$=0.242×V_{BAT}; t_{bit}=96μs; V_{BAT}=6.1V~7.6V Fig 6			0.590	
Timing characteristics						
receiver propagation delay	$t_{PD(RX)}$ [4]				6	μs
receiver propagation delay symmetry	$t_{PD(RX)sym}$ [4]		-2		2	μs
LIN dominant wake-up time	$t_{wake(dom)LIN}$	Sleep mode	30	65	150	μs
dominant wake-up time on pin WAKE_N	$t_{wake(dom)WAKE\_N}$	Sleep mode	7	22	50	μs
go to normal time	$t_{gotonorm}$		2	5	10	μs
go to sleep time	$t_{gotosleep}$		2	5	10	μs
TXD dominant time-out time	$t_{to(dom)TXD}$	V_{TXD}=0V	27	52	90	ms

(Unless specified otherwise; 5.5V≤V_{BAT}≤27V, -40°C≤T_j≤150°C; typical in V_{BAT}=12V, T_j=25°C.)

[1] $\delta 1, \delta 3 = \frac{t_{bus(rec)(\min)}}{2 \times t_{bit}}$.

[2] Bus load conditions are: (1) C_L=1nF, R_L=1kΩ; (2) C_L=6.8nF, R_L=660Ω; (3) C_L=10nF, R_L=500Ω.

[3] $\delta 2, \delta 4 = \frac{t_{bus(rec)(\max)}}{2 \times t_{bit}}$.

[4] Load condition pin RXD: C_{TXD}=20pF, R_{RXD}=2.4kΩ.

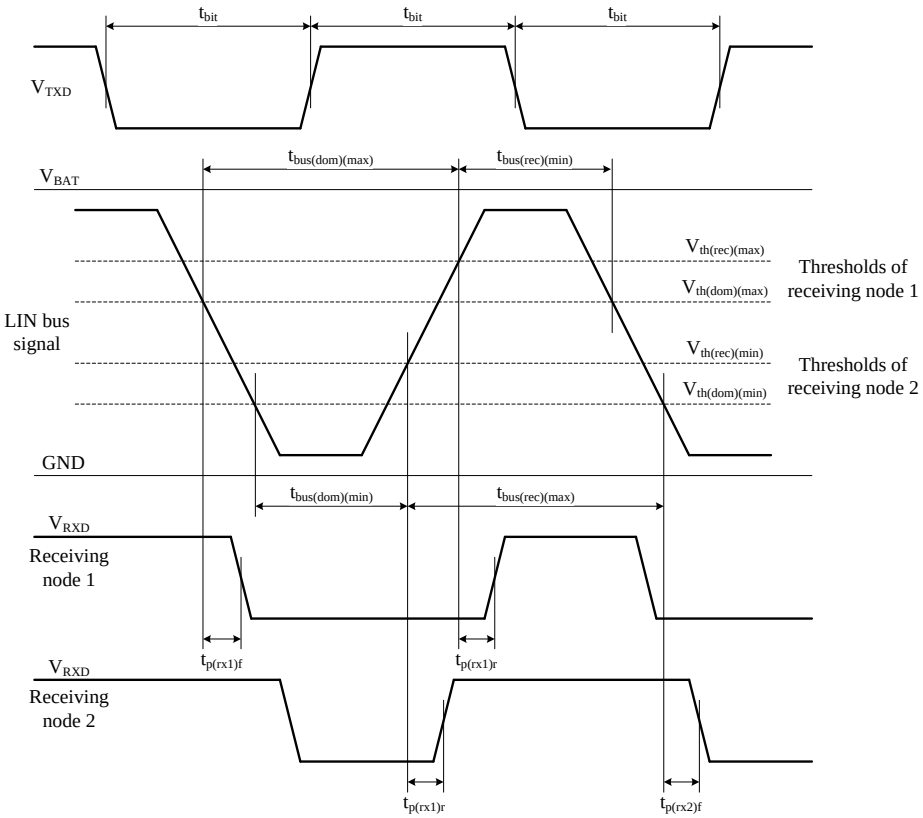


Fig 6. Timing diagram LIN transceiver

TYPICAL APPLICATION

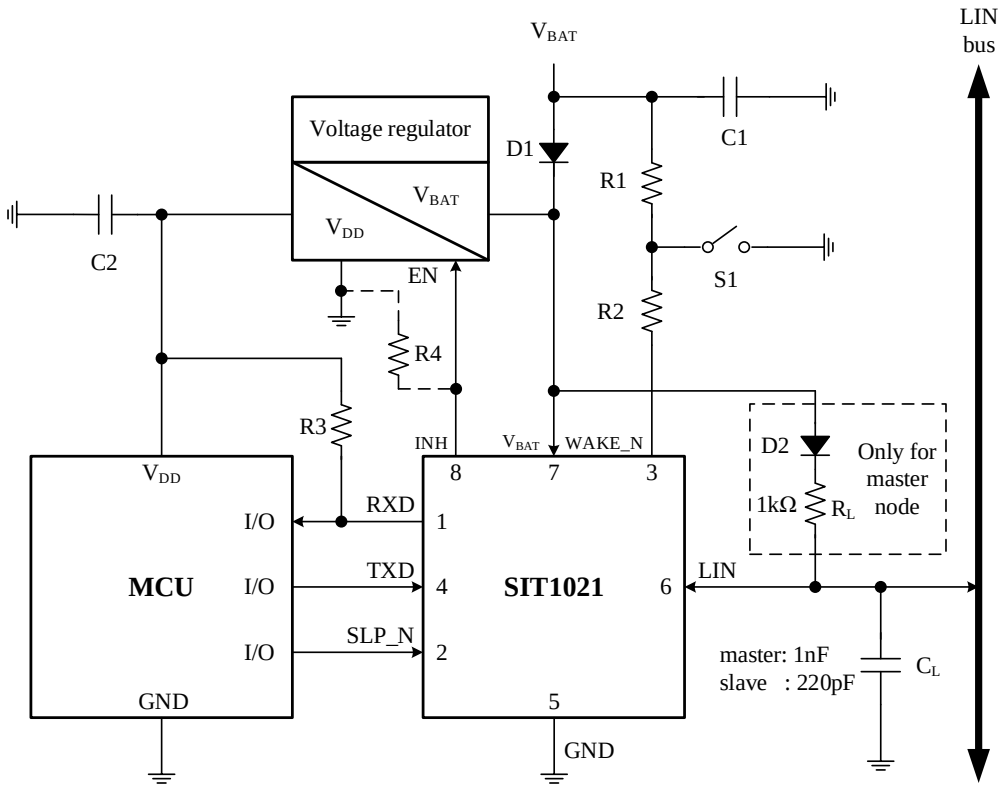


Fig 7. Typical application of the SIT1021

Note: To obtain a slower bus waveform slope, it is recommended to use a R_L/C_L combination of 660Ω/6.8nF, where R_L/C_L is the equivalent value of all nodes summarized. R4 (10kΩ~100kΩ) is the drop-down resistance from INH to GND. Whether to add the pull-down resistance and its value should be selected according to the status of the EN pin of the external power supply chip.

TIMING TEST CIRCUIT

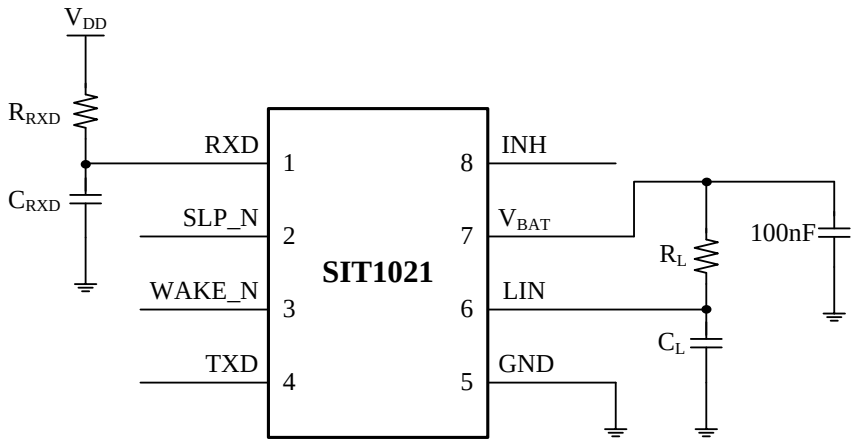
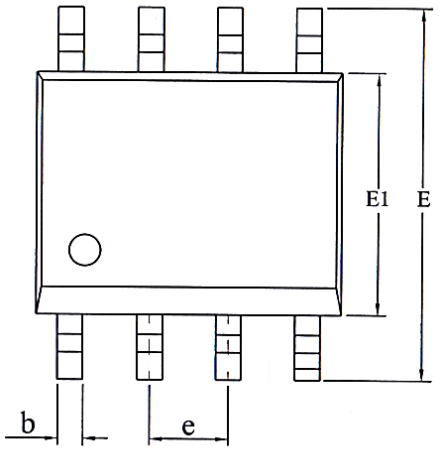


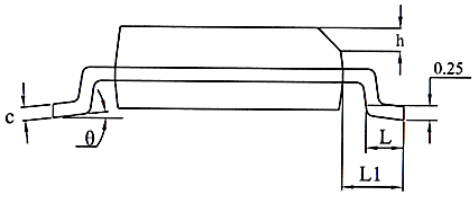
Fig 8. Timing test circuit for LIN transceiver

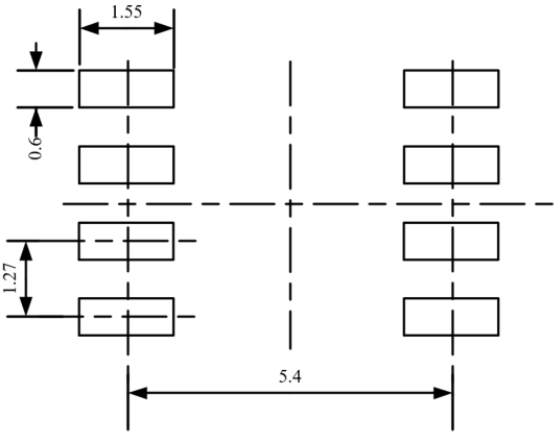
SOP8 DIMENSIONS

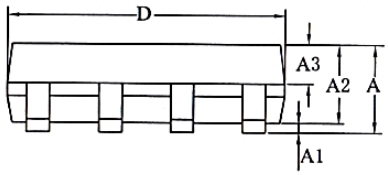
PACKAGE SIZE

SYMBOL	MIN./mm	TYP./mm	MAX./mm
A	1.40	-	1.80
A1	0.10	-	0.25
A2	1.30	1.40	1.50
A3	0.60	0.65	0.70
b	0.38	-	0.51
D	4.80	4.90	5.00
E	5.80	6.00	6.20
E1	3.80	3.90	4.00
e	1.27BSC		
h	0.25	-	0.50
L	0.40	0.60	0.80
L1	1.05REF		
c	0.20	-	0.25
θ	0°	-	8°







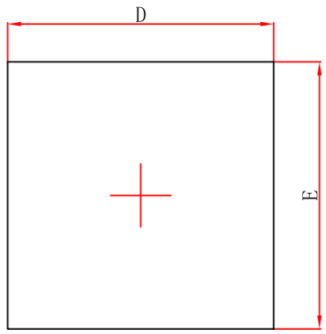


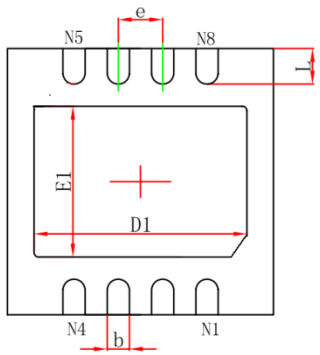
LAND PATTERN EXAMPLE (Unit: mm)

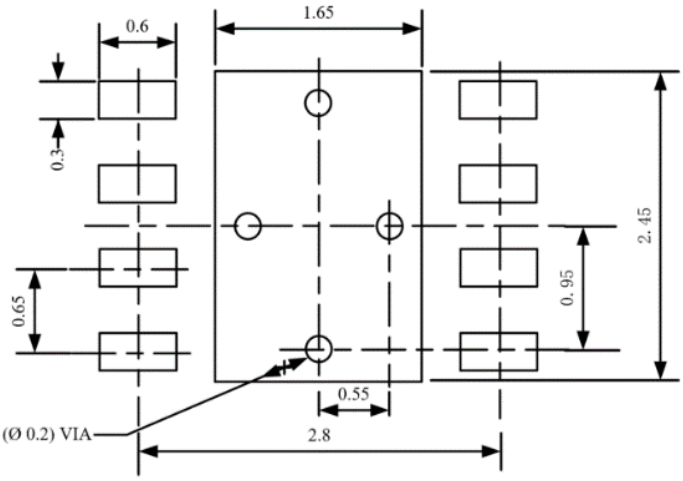
DFN3*3-8 DIMENSIONS

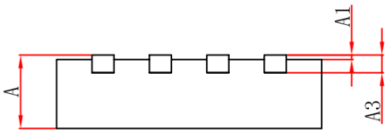
PACKAGE SIZE

SYMBOL	MIN./mm	TYP./mm	MAX./mm
A	0.70		0.80
A1	0.00	0.02	0.05
A3	0.203 REF		
D	2.90	3.00	3.10
E	2.90	3.00	3.10
D1	2.35	2.45	2.55
E1	1.55	1.65	1.75
b	0.2	0.25	0.33
e	0.65 TYP		
L	0.35		0.45



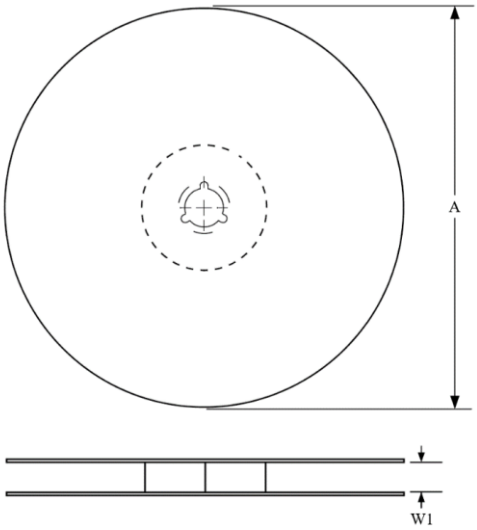




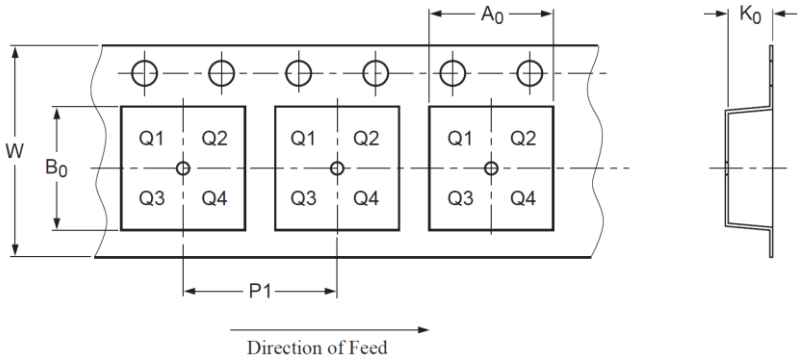


LAND PATTERN EXAMPLE (Unit: mm)

TAPE AND REEL INFORMATION



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers



PIN1 is in quadrant 1

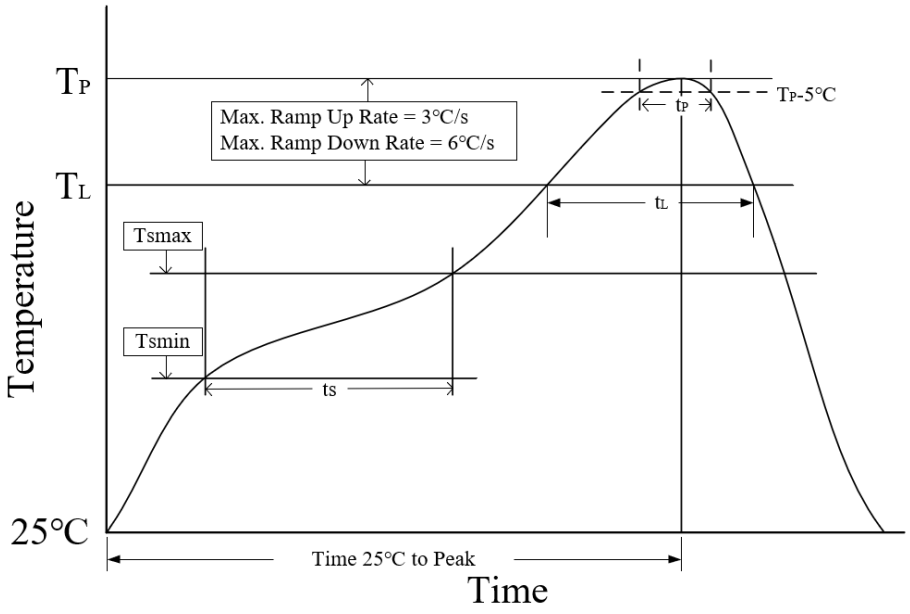
封装类型	卷盘直径 A (mm)	编带宽度 W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)
SOP8	330±1	12.4	6.60±0.1	5.30±0.10	1.90±0.1	8.00±0.1	12.00±0.1
DFN3*3-8	329±1	12.4	3.30±0.1	3.30±0.1	1.10±0.1	8.00±0.1	12.00±0.3

ORDERING INFORMATION

TYPE NUMBER	PACKAGE	PACKING
SIT1021T	SOP8	Tape and reel
SIT1021TK	DFN3*3-8， Small shape, no leads	Tape and reel

SOP8 is packed with 2500 pieces/disc in braided packaging. Leadless DFN3*3-8 is packed with 5000 pieces/disc in braided packaging.

REFLOW SOLDERING



Parameter	Lead-free soldering conditions
Ave ramp up rate (T_L to T_P)	3 °C/second max
Preheat time ts (T_{smin}=150 °C to T_{smax}=200 °C)	60-120 seconds
Melting time t_L (T_L=217 °C)	60-150 seconds
Peak temp T_P	260-265 °C
5°C below peak temperature t_P	30 seconds
Ave cooling rate (T_P to T_L)	6 °C/second max
Normal temperature 25°C to peak temperature T_P time	8 minutes max

Important statement

SIT reserves the right to change the above-mentioned information without prior notice.

REVISION HISTORY

Version number	Data sheet status	Revision date
V1.0	Initial version.	July 2020
V1.1	Add the internal block diagram of SIT1021; Modify the state transition diagram; Modify the remote wake-up sequence diagram.	January 2021
V1.2	Added ESD test model description; Modify the range of the IBAT indicator; Modify the $I_{BUS\_PAS\_rec}$ indicator range; Modify the $I_{L(lob)}$ indicator range; Correct the temperature range.	April 2021
V1.3	Modify the limit parameter index; Modify the range of the I_{BAT} indicator; Modify the range of V_{BAT} power-on and power-off threshold indicators; Modify the range of the I_{BUS_PAS}_dom indicator; Modify the $I_{BUS\_NO\_GND}$ indicator range; Modify the R_{slave} indicator range.	August 2021
V1.4	Modified the range of $V_{th(BAT)H}$ indicator; Added SIT1021 typical application load combination description.	November 2021
V1.5	Modified package size information.	January 2022
V1.6	Added “LAND PATTERN EXAMPLE”; Added tape information; Added reflow information.	April 2022
V1.7	Updated ordering information； Updated typical application diagram and added related application descriptions.	January 2023