FEATURE

- Compliant with LIN 2.x/ISO 17987-4:2016 (12V)/SAE J2602
- Compatible with K line
- Integrated over-temperature protection function (thermal shutdown)
- Integrated dominant time out function
- Integrated bus pull-up slave termination resistor
- Bus current limiting protection
- Supply undervoltage detection
- Very low power consumption sleep mode and standby mode
- Support LIN bus remote wake-up
- LIN data transmission rate up to 20kbps
- Available in SOP14 and DFN4.5×3-14 packages

PRODUCT APPEARANCE

Fig 1. Provide environmentally friendly lead-free package

DESCRIPTION

SIT1022Q is a dual channel Local Interconnect Network (LIN) physical layer transceiver that compliant with LIN 2.0, LIN 2.1, LIN 2.2, LIN 2.2A, ISO 17987-4:2016 (12V) and SAE J2602 standards. It is mainly suitable for in-vehicle networks with a transmission rate of 1kbps to 20kbps. SIT1022Q controls the state of the LINx bus through the TXDx pin, and can convert the data stream sent by the protocol controller into a bus signal with the best slew rate and waveform shaping to minimize electromagnetic radiation emission (EME). The LIN bus output pin has an internal pull-up resistor. Only when used as a master node, the LIN bus port needs to be pulled up to V_{BAT} through an external resistor in series with a diode. SIT1022Q receives the data stream on the bus through the LINx pin, and transmits the data to the external microcontroller through the receiver's output pin RXDx.

SIT1022Q can operate from 5.5V to 18V and supports 12V applications. SIT1022Q has an extremely low quiescent current consumption in sleep mode and standby mode. It can quickly minimize power consumption in the event of a failure. The device can be placed in normal mode via a signal on the pin SLP_Nx.

PIN CONFIGURATION

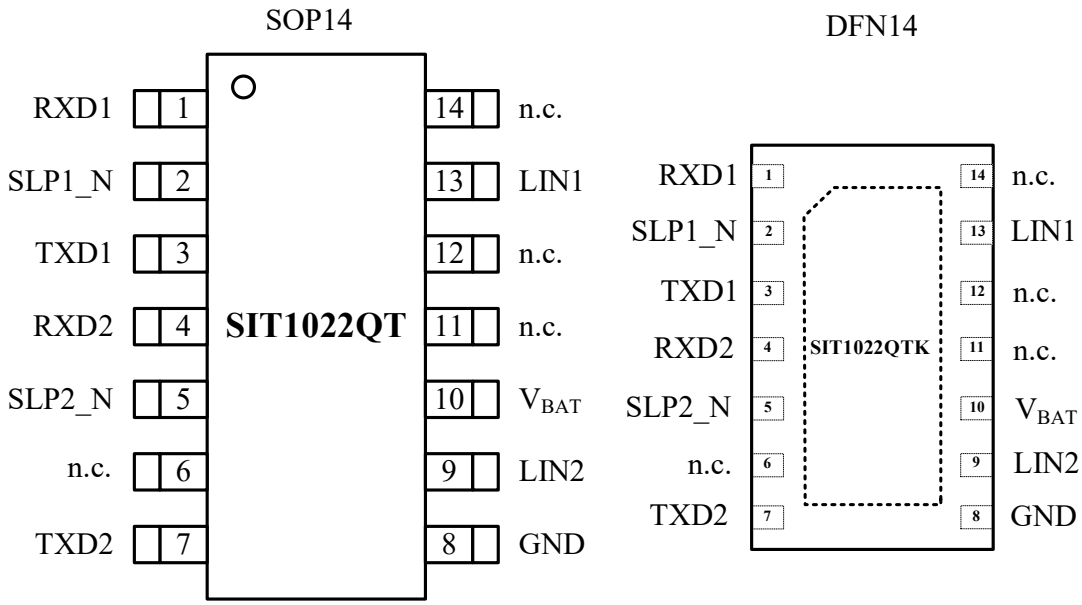


Fig 2. SIT1022Q pin configuration diagram

PIN DESCRIPTION

Table 1. SIT1022Q pin description

Pin	Symbol	Description
1	RXD1	receive data output 1(open-drain); active LOW after a wake-up event.
2	SLP1_N	enable input 1, high level enables devices into Normal mode, low level enables devices Sleep mode, reset the wake-up request on RXD1
3	TXD1	transmit data input 1
4	RXD2	receive data output 2(open-drain); active LOW after a wake-up event.
5	SLP2_N	enable input 2, high level enables devices into Normal mode, low level enables devices Sleep mode, reset the wake-up request on RXD2
6	n.c.	not connected
7	TXD2	transmit data input 2
8	GND	ground
9	LIN2	LIN bus line 2 input/output
10	V_{BAT}	battery supply voltage

Pin	Symbol	Description
11	n.c.	not connected
12	n.c.	not connected
13	LIN1	LIN bus line 1 input/output
14	n.c.	not connected

NOTE: In the DFN4.5×3-14 package, the pad on the back is connected to the GND pin of the chip. In order to obtain better heat dissipation performance, the pad on the back can be connected to a suitable "ground" on the PCB board.

BLOCK DIAGRAM

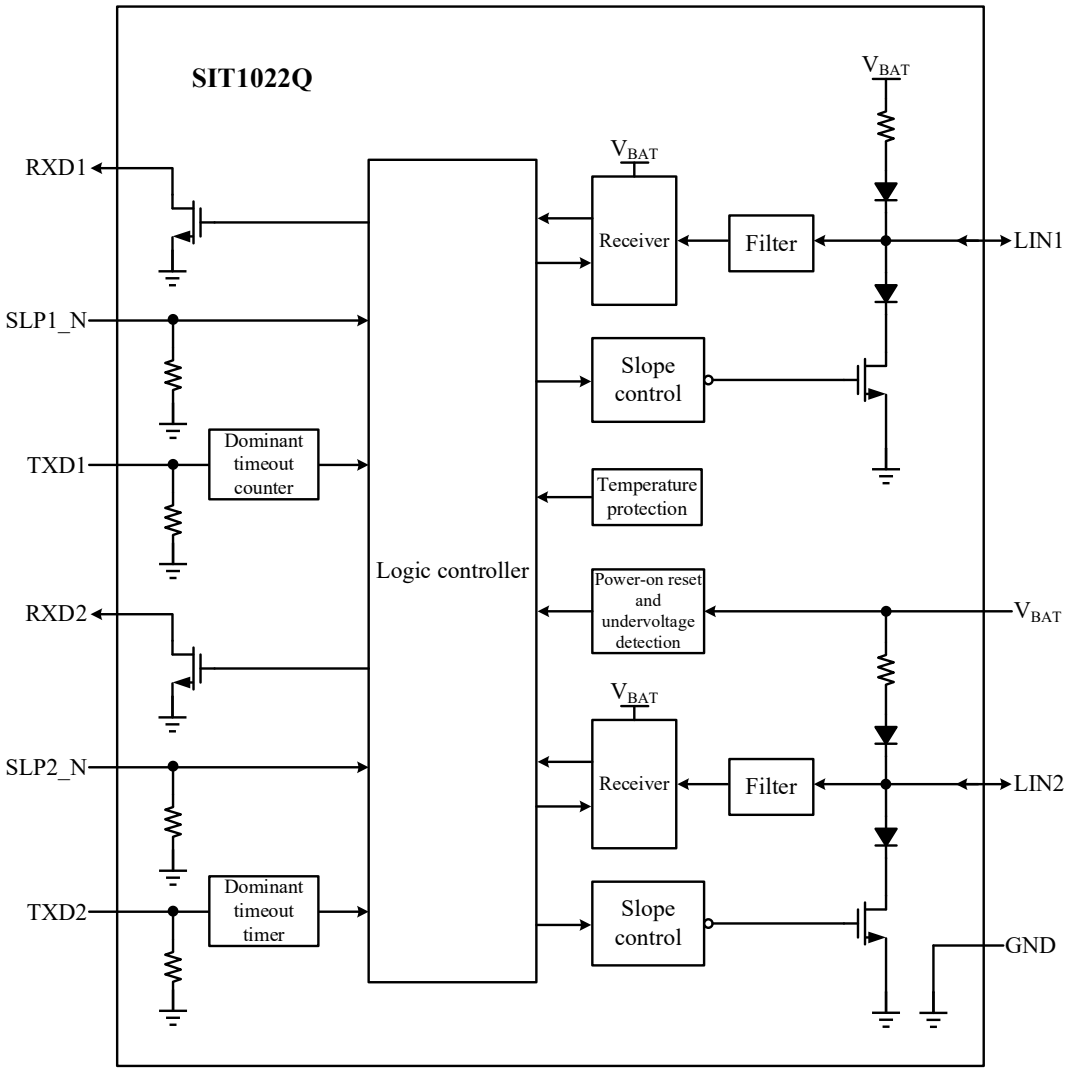


Fig 3. Block diagram of SIT1022Q

FEATURE DESCRIPTION

1 Overview

The SIT1022Q is a dual channel interface chip used between the LIN protocol controller and the physical bus. It can be used in trucks, buses, cars and industrial control with a data rate up to 20kbps. The SIT1022Q receives the data stream sent by protocol controller at the pin TXDx, and converts it into a bus signal with appropriate slew rate and waveform shaping. The input data on LIN bus is output to external microcontroller by pin RXDx. This device is compliant with LIN 2.0, LIN 2.1, LIN 2.2, LIN 2.2A, ISO 17987-4:2016 (12V) and SAE J2602 standards.

2 Operating modes

As shown in Fig 4, the SIT1022Q supports four functional modes for very-low-power operation (Sleep mode), standby operation (Standby mode), normal operation (Normal mode) and power-up (Power-on reset mode). The operating states in each mode are shown in Table 2. The SIT1022Q is a dual-channel LIN transceiver. Except for the power-on reset mode, the working state of each channel can be controlled independently, that is, the LIN transceiver of the two channels can work in different modes respectively.

2.1 Sleep Mode

In normal mode, when SLPx_N pin has a falling edge and SLPx_N remains low for longer than $t_{gotosleep}$, the LIN transceiver of the corresponding channel of SIT1022Q enters the sleep mode. The SIT1022Q has very low static power consumption when both LIN transceivers of dual channels enter hibernation mode, but it can still remotely wake up the corresponding channel to enter standby mode through LINx pin, or directly switch to normal mode by pulling up SLPx_N pin.

In order to prevent the SIT1022Q from waking up due to unexpected wake up events caused by car transient or EMI, filters are designed at the inputs LINx pin and SLPx_N pin of the receiver. The necessary conditions for SIT1022Q to be woken up in sleep mode are as follows: the remote wake-up time through LINx pin must be greater than $t_{wake(dom)LIN}$ (dominant wake time of bus); The direct wake-up time through the SLPx_N pin must be longer than the $t_{gotonorm}$.

2.2 Standby Mode

When SIT1029Q is in sleep mode, if a remote wake-up event is detected, the device will automatically enter standby mode immediately, and the low level on the RXDx pin will indicate that the wake-up process is used to send an wake up source flag to the MCU. The SIT1022Q has very low static power consumption when both dual-channel LIN transceivers are in standby mode.

Setting pin SLPx_N high during standby mode may result in the following events:

(1) The LIN transceiver of the corresponding channel enters the normal mode if the high level on pin SLPx_N has been maintained for a certain time period ($t_{gotonorm}$).

(2) An immediate reset of the wake-up request signal on pin RXDx.

2.3 Normal Mode

Only in normal mode the SIT1022Q is able to transmit and receive data via the LIN bus and the communication of dual channel LIN transceiver operates independently. The receiver detects the data stream on the LIN bus and outputs it to the microcontroller via pin RXDx, and the high level of bus represents recessive and low level represents dominant. Normal mode is entered as a high level on pin SLP_N and maintained for a time of at least $t_{gotonorm}$ while the SIT1029Q is in Sleep or Standby mode. The Sleep mode is entered by setting pin SLP_N low for longer than $t_{gotosleep}$. TXDx is the output of the driver, the data stream from protocol controller sent by TXDx to LINx pin output and waveform shaping to minimize electromagnetic radiation emission (EME). When SIT1022Q is used as slave node, LINx port is pulled to V_{BAT} via internal slave resistor. When the SIT1022Q is used as the host node, the LINx port is pulled up to the V_{BAT} through an external resistor and a diode in series.

In sleep or standby mode, as long as the high level hold time on the SLPx_N pin is longer than the $t_{gotonorm}$, the LIN transceiver of the corresponding channel will enter the normal mode. If the low level hold time on the SLPx_N pin is greater than $t_{gotosleep}$, the LIN transceiver on the corresponding channel switches to sleep mode.

2.4 Power-on Reset Mode

If the voltage on V_{BAT} is less than the low-level reset threshold $V_{th(VBATL)L}$ when powering on, the SIT1022Q is in power-on reset mode and all input and output functions are disabled; when the voltage on V_{BAT} is greater than the high-level reset threshold $V_{th(VBAT)H}$, SIT1022Q enters sleep mode.

3 Remote Wake Up Events

LINx pin remote wake-up: When the LINx pin is pulled down to a low level through a falling edge, a rising edge appears at the next moment, and the low-level holds time between the rising edge and the falling edge at the previous moment is greater than $t_{wake(dom)LIN}$, the process is regarded as effective remote wake-up (as shown in Fig 5). After the remote wake-up, the wake-up request event interrupts the microcontroller with the low level of the RXDx pin as the indicator signal.

4 Thermal Shutdown

In normal mode, the over-temperature protection circuit will disable the output driver when the junction temperature of SIT1022Q exceeds the shutdown junction temperature $T_{j(sd)}$. When the junction temperature is lower than the hysteresis temperature, the driver is enabled again.

5 Dominant Timeout Function

If the TXD pin is forced to be permanently low due to hardware and/or software application failures, the integrated TXD dominant timeout timer circuit prevents the bus line from being driven to a permanently dominant state (blocking all network communications). The timer is triggered by the falling edge on the TXD pin. If the low level on the TXD pin holds longer than the internal timer time ($t_{to(dom)TXD}$), the transmitter will be disabled and the drive bus will go into a recessive state. The timer is reset by the rising edge on the TXD pin.

6 Fail-safe Feature

➢ The interior of the TXD pin is pulled down to the ground to prevent the undefined floating state of the TXD pin

➢ The interior of the SLPx_N pin is pulled down to the ground, and the corresponding LIN transceiver will enter the sleep mode when the SLPx_N pin is floating.

➢ The loss-of-ground condition has no effect on the bus port, and the bus port has no reverse current

➢ The bus driver output stage current limiting to prevent the driver from burning down or functional effects when the bus short-circuits to the V_{BAT}.

➢ To avoid the effects caused by TXD pins being forced to permanently low due to hardware and/or software application failures, after switching to normal mode, the LIN driver will be enabled only if a high TXD level is detected.

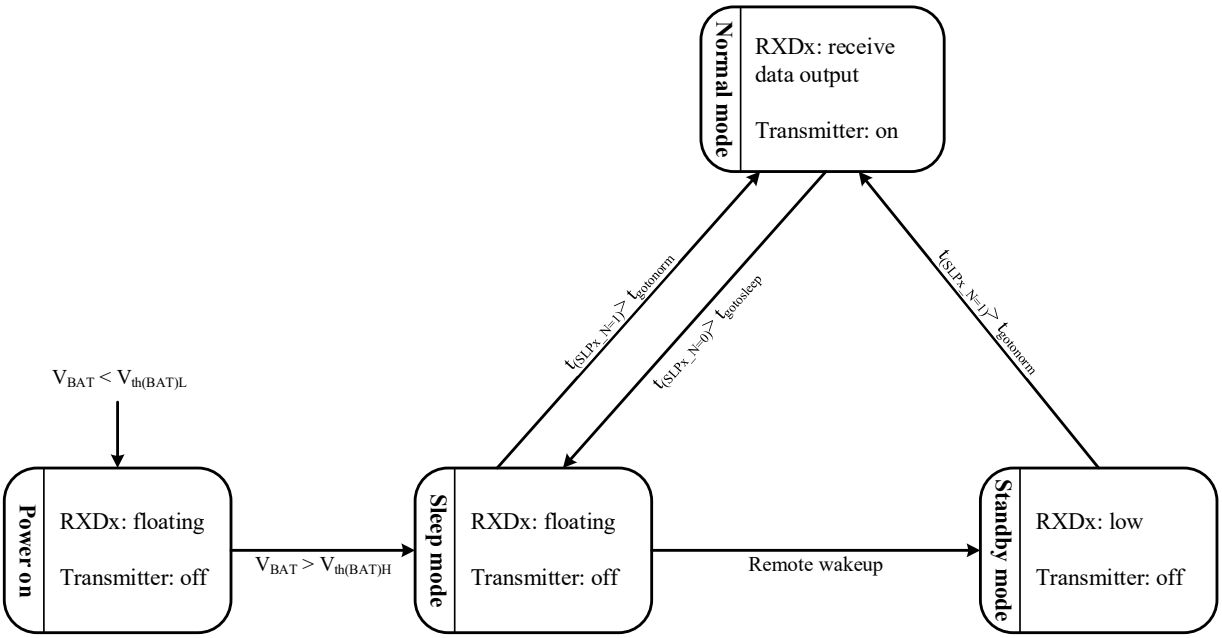


Fig 4. State diagram

Table 2. Working status of SIT1022Q in each mode

Mode	SLPx_N	RXDx	Transmitter x	Remarks
Sleep x	low	floating	off	no wake-up request detected
Standby x	low	low	off	wake-up request detected
Normal x	high	recessive: high dominant: low	on	Enable bus signal shaping
Power-on	low	floating	off	Disable all input and output functions

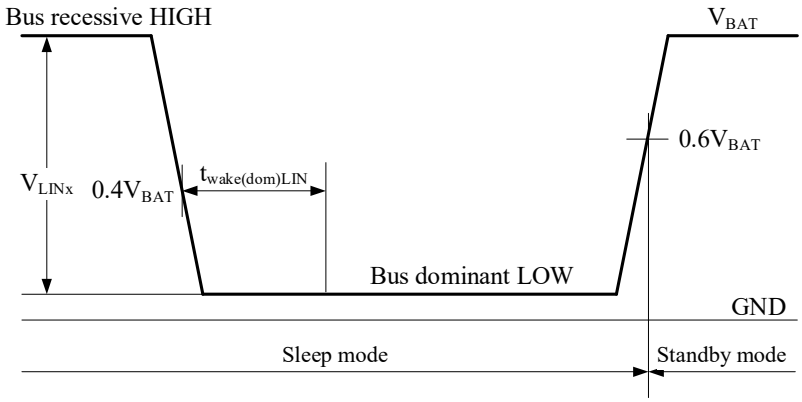


Fig 5. Remote wake-up behavior

LIMITING VALUES

Parameter	Symbol	Conditions	Range	Unit
battery supply voltage	V_{BAT}	with respect to GND	-0.3 ~ +42	V
voltage on pin TXD	V_{TXD}	TXD1 and TXD2	-0.3 ~ +7	V
voltage on pin RXD	V_{RXD}	RXD1 and RXD2	-0.3 ~ +7	V
voltage on pin SLP_N	V_{SLP_N}	SLP1_N and SLP2_N	-0.3 ~ +7	V
voltage on pin LIN	V_{LIN}	LIN1 and LIN2, with respect to GND	-42 ~ +42	V
virtual junction temperature	T_j		-40 ~ +150	°C
storage temperature	T_{stg}		-55 ~ +150	°C

NOTE: The maximum limit parameters mean that exceeding these values may cause irreversible damage to the device. Under these conditions, it is not conducive to the normal operation of the device. The continuous operation of the device at the maximum allowable rating may affect the reliability of the device. The reference point for all voltages is ground.

STATIC CHARACTERISTICS

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Power consumption						
battery supply voltage	V_{BAT}		5.5		18	V
battery supply current	I_{BAT}	Sleep mode (dual channel); bus recessive (binary channels); $V_{LINx}=V_{BAT}$; $V_{SLPx\_N}=0V$	-	6	15	μA
		Sleep mode (dual channel); bus dominant (dual channel); $V_{LINx}=0V$; $V_{SLPx\_N}=0V$	-	800	2000	μA
		Standby mode (dual channel); bus recessive (dual channel); $V_{LINx}=V_{BAT}$; $V_{SLPx\_N}=0V$	-	6	15	μA
		Standby mode (dual channel); bus dominant (dual channel); $V_{BAT}=12V$; $V_{LINx}=0V$; $V_{SLPx\_N}=0V$	-	800	2000	μA
		Normal mode (dual channel); bus recessive (dual channel); $V_{LINx}=V_{BAT}$; $V_{TXDx}=5V$; $V_{SLPx\_N}=5V$	-	240	800	μA
		Normal mode (dual channel); bus dominant (dual channel); $V_{BAT}=12V$; $V_{TXDx}=0V$; $V_{SLPx\_N}=5V$	-	3	8	mA

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Power-on reset						
LOW-level V_{BAT} reset threshold voltage	$V_{th}(V_{BATL})L$		3.9	4.4	4.7	V
HIGH-level V_{BAT} reset threshold voltage	$V_{th}(V_{BATL})H$		4.2	4.7	5.1	V
V_{BAT} reset hysteresis voltage	$V_{hys}(V_{BATL})$ [1]		0.15	0.3	0.6	V
Pin TXDx						
HIGH-level input voltage	V_{IH}		2	-	7	V
LOW-level input voltage	V_{IL}		-0.3	-	+0.8	V
hysteresis voltage	V_{hys} [1]		50	200	400	mV
pull-down resistance on pin TXDx	$R_{PD(TXDx)}$	V_{TXDx}=5V	50	125	400	kΩ
LOW-level input current	I_{IL}	V_{TXDx}=0V	-5	-	5	μA
Pin SLPx_N						
HIGH-level input voltage	V_{IH}		2	-	7	V
LOW-level input voltage	V_{IL}		-0.3	-	0.8	V
hysteresis voltage	V_{hys} [1]		50	200	400	mV
pull-down resistance on pin SLPx_N	$R_{PD(SLPx\_N)}$	V_{SLPx_N}=5V	100	250	650	kΩ
LOW-level input current	I_{IL}	V_{SLPx_N}=0V	-5	-	5	μA
Pin RXDx						
LOW-level output current	I_{OL}	Normal mode; V_{RXDx}=0.4V; V_{LINx}=0V	2	-	-	mA
HIGH-level leakage current	I_{LH}	Normal mode; V_{RXDx}=5V; V_{LINx}=V_{BAT}	-5	-	5	μA
Pin LINx						
current limitation for driver dominant state	I_{BUS_LIM}	V_{TXDx}=0V; V_{LINx}=V_{BAT}=18V	40	-	100	mA

Parameter	Symbol	Condition	Min	Typ	Max	Unit
receiver recessive input leakage current	$I_{BUS\_PAS\_rec}$	V_{TXDx}=5V; V_{LINx}=18V; V_{BAT}=5.5V	-	-	5	μA
receiver dominant input leakage current	$I_{BUS\_PAS\_dom}$	Normal mode; V_{TXDx}=5V; V_{LINx}=0V; V_{BAT}=12V	-600	-	-	μA
loss-of-ground bus current	$I_{BUS\_NO\_GND}$	V_{BAT}=18V; V_{LINx}=0V	-1000	-	10	μA
loss-of-ground bus current	$I_{BUS\_NO\_BAT}$	V_{BAT}=0V; V_{LINx}=18V	-	-	5	μA
Receiver dominant threshold voltage	$V_{th(dom)RX}$		-	-	$0.4V_{BAT}$	V
Receiver recessive threshold voltage	$V_{th(rec)RX}$		$0.6V_{BAT}$	-	-	V
Receiver center voltage	$V_{th(RX)cntr}$	$V_{th(RX)\ cntr}$= ($V_{th(rec)RX}$+ $V_{th(dom)RX}$)/2	$0.475V_{BAT}$	0.5 V_{BAT}	$0.525V_{BAT}$	V
receiver hysteresis threshold voltage	$V_{th(hys)RX}$	$V_{th(hys)RX}$= $V_{th(rec)RX}$-$V_{th(dom)RX}$	-	-	$0.175V_{BAT}$	V
slave resistance	R_{slave}	connected between pins LIN and V_{BAT}; V_{LINx}=0V; V_{BAT}=12V; V_{TXDx}=V_{SLPx_N}=5V	20	30	60	kΩ
capacitance on pin LIN	C_{LIN} [1]		-	-	20	pF
dominant output voltage	$V_{o(dom)}$	Normal mode; V_{TXDx}=0V; V_{BAT}=7V	-	-	1.4	V
		Normal mode; V_{TXDx}=0V; V_{BAT}=18V	-	-	2.0	V
Thermal shutdown						
shutdown junction temperature	$T_{j(sd)}$ [1]		150	-	200	°C

(Unless specified otherwise; 5.5V≤V_{BAT}≤18V, -40°C≤T_j≤150°C; typical in V_{BAT}=12V, T_{amb}=25°C.)

[1] Not tested in production; guaranteed by design.

SWITCH CHARACTERISTICS

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Duty cycles						
Duty cycle 1	$\delta 1$ [1][2]	$V_{th(rec)(max)}=0.744\times V_{BAT}$; $V_{th(dom)(max)}=0.581\times V_{BAT}$; $t_{bit}=50\mu s$; $V_{BAT}=7V\sim18V$ Fig 6	0.396	-	-	
		$V_{th(rec)(max)}=0.76\times V_{BAT}$; $V_{th(dom)(max)}=0.593\times V_{BAT}$; $t_{bit}=50\mu s$; $V_{BAT}=5.5V\sim7V$ Fig 6	0.396	-	-	
Duty cycle 2	$\delta 2$ [2][3]	$V_{th(rec)(min)}=0.422\times V_{BAT}$; $V_{th(dom)(min)}=0.284\times V_{BAT}$; $t_{bit}=50\mu s$; $V_{BAT}=7.6V\sim18V$ Fig 6	-	-	0.581	
		$V_{th(rec)(min)}=0.41\times V_{BAT}$; $V_{th(dom)(min)}=0.275\times V_{BAT}$; $t_{bit}=50\mu s$; $V_{BAT}=6.1V\sim7.6V$ Fig 6	-	-	0.581	
Duty cycle 3	$\delta 3$ [1][2]	$V_{th(rec)(max)}=0.778\times V_{BAT}$; $V_{th(dom)(max)}=0.616\times V_{BAT}$; $t_{bit}=96\mu s$; $V_{BAT}=7V\sim18V$ Fig 6	0.417	-	-	
		$V_{th(rec)(max)}=0.797\times V_{BAT}$; $V_{th(dom)(max)}=0.630\times V_{BAT}$; $t_{bit}=96\mu s$; $V_{BAT}=5.5V\sim7V$ Fig 6	0.417	-	-	
Duty cycle 4	$\delta 4$ [2][3]	$V_{th(rec)(min)}=0.389\times V_{BAT}$; $V_{th(dom)(min)}=0.251\times V_{BAT}$; $t_{bit}=96\mu s$; $V_{BAT}=7.6V\sim18V$ Fig 6	-	-	0.590	
		$V_{th(rec)(min)}=0.378\times V_{BAT}$; $V_{th(dom)(min)}=0.242\times V_{BAT}$; $t_{bit}=96\mu s$; $V_{BAT}=6.1V\sim7.6V$ Fig 6	-	-	0.590	
Timing characteristics						
receiver propagation delay	$t_{PD(RX)}$ [4]		-	-	6	μs
receiver propagation delay symmetry	$t_{PD(RX)sym}$ [4]		-2	-	2	μs

Parameter	Symbol	Condition	Min	Typ	Max	Unit
LIN dominant wake-up time	$t_{wake(dom)LIN}$	Sleep mode	30	68	150	μs
go to normal time	$t_{gotonorm}$		2	5	10	μs
go to sleep time	$t_{gotosleep}$		2	5	10	μs
Dominant time-out time	$t_{to(dom)TXD}$	start with the falling edge on TXDx	6	12	50	ms

(Unless specified otherwise; 5.5V≤V_{BAT}≤18V, -40°C≤T_j≤150°C; typical in V_{BAT}=12V, T_{amb}=25°C.)

[1] $\delta 1, \delta 3 = \frac{t_{bus(rec)(\min)}}{2 \times t_{bit}}$;

[2] Bus load conditions: (1) C_{Lx}=1nF, R_{Lx}=1kΩ; (2) C_{Lx}=6.8nF, R_{Lx}=660Ω; (3) C_{Lx}=10nF, R_L=500Ω;

[3] $\delta 2, \delta 4 = \frac{t_{bus(rec)(\max)}}{2 \times t_{bit}}$;

[4] Load condition pin RXDx: C_{RXDx}=20pF, R_{RXDx}=2.4kΩ.

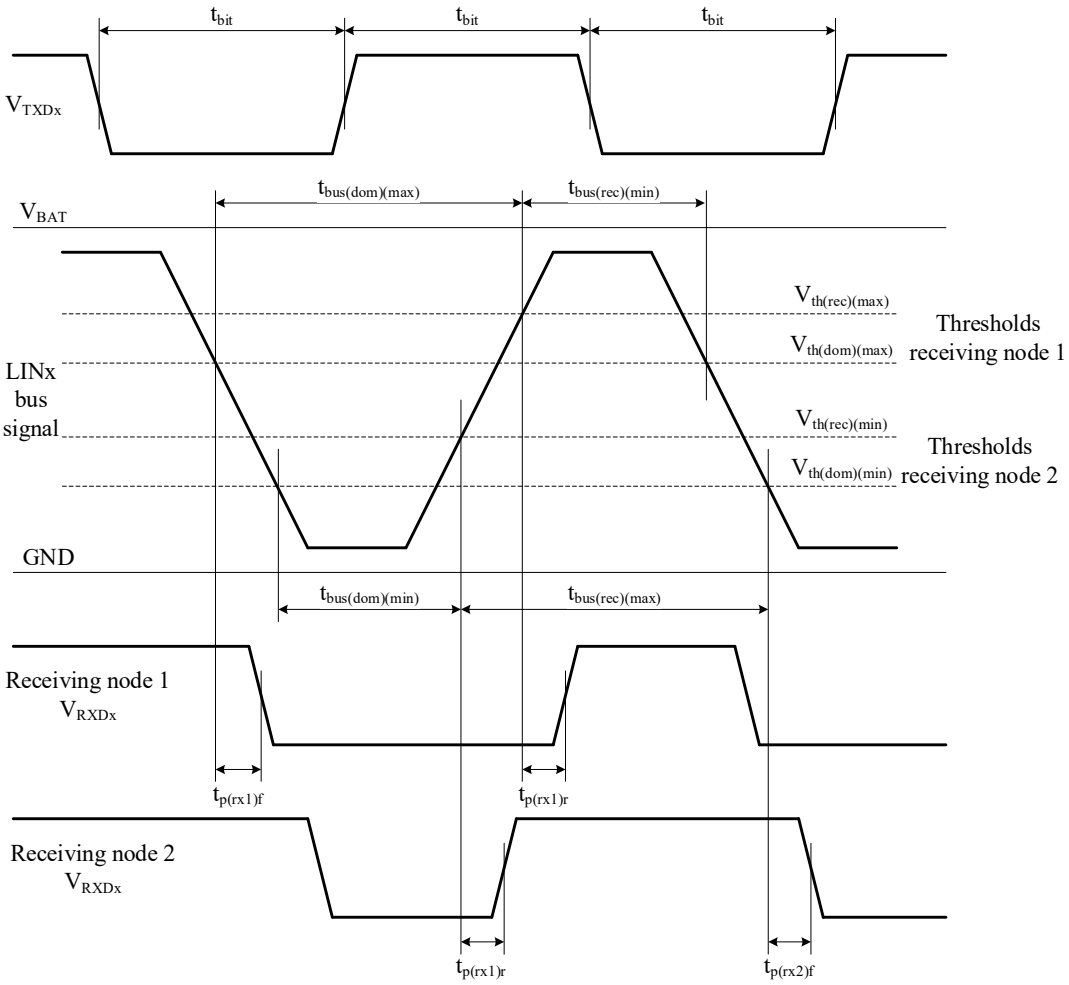


Fig 6. Bus signal transmission timing diagram

TYPICAL APPLICATION

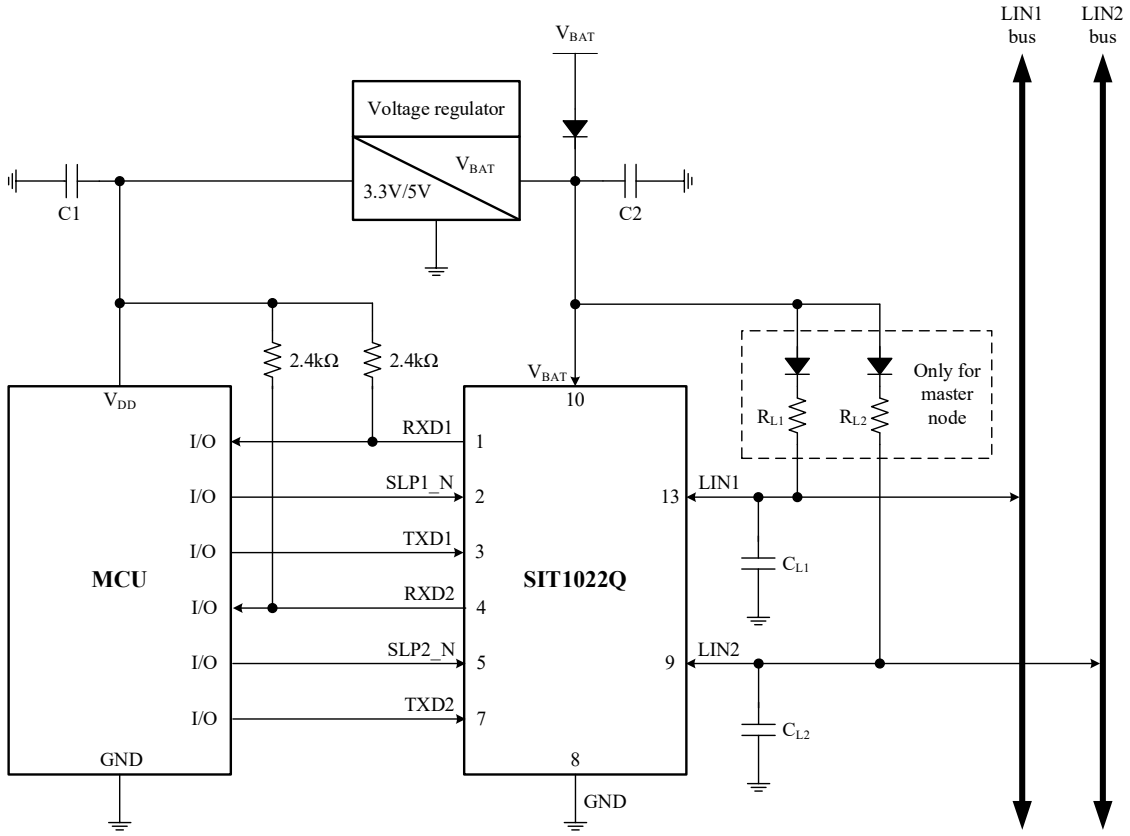


Fig 7. Typical application of the SIT1022Q

Note: R_{Lx}/C_{Lx} combination of 660Ω/6.8nF is recommended when the master node is used to obtain a slower bus waveform slope.

TIMING TEST CIRCUIT

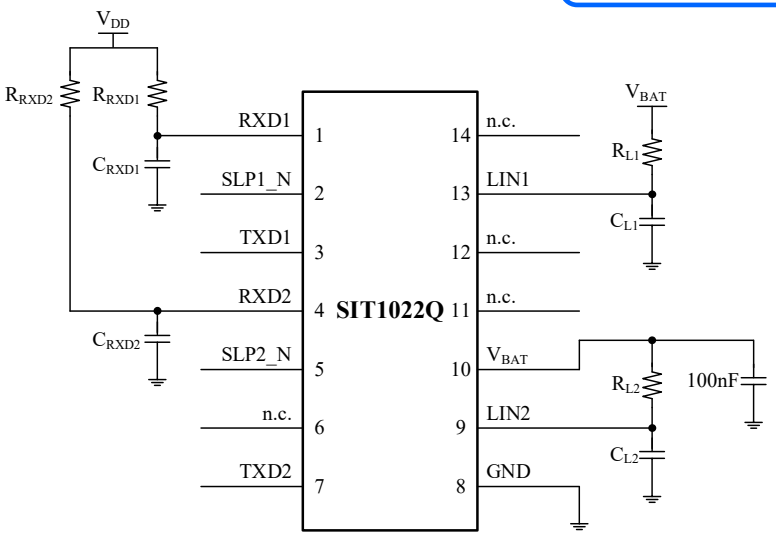
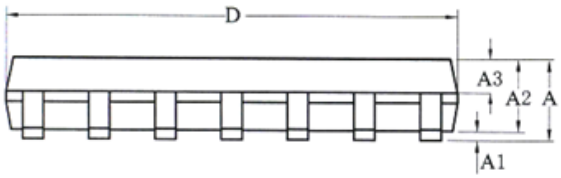


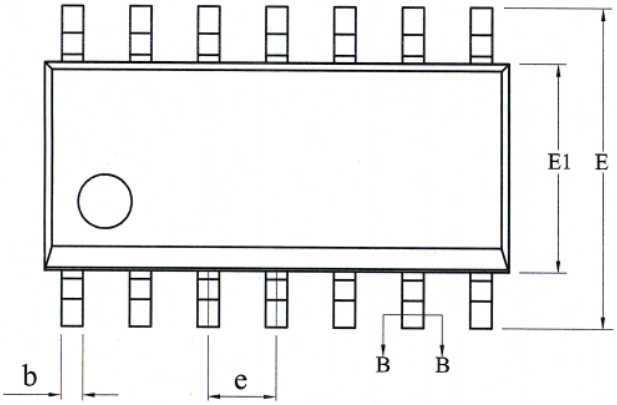
Fig 8. Switch characteristics test circuit

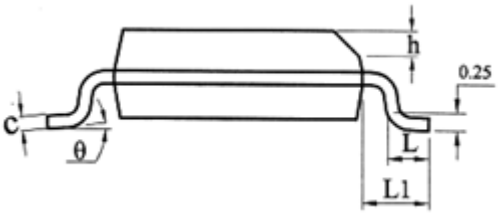
SOP14 DIMENSIONS

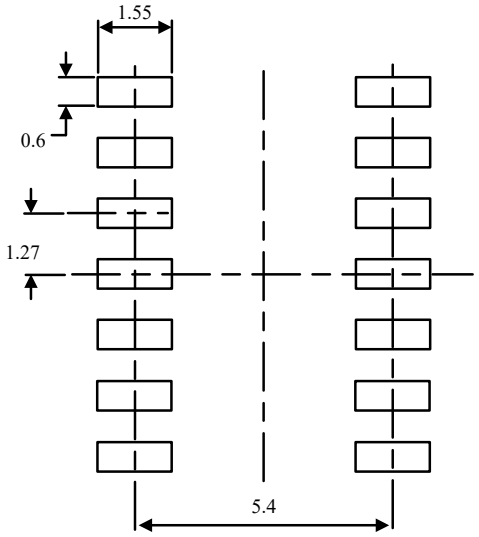
PACKAGE SIZE

Symbol	Min./mm	Typ./mm	Max./mm
A	-	-	1.75
A1	0.10	-	0.225
A2	1.30	1.40	1.50
A3	0.60	0.65	0.70
b	0.39	-	0.47
b1	0.38	0.41	0.44
c	0.20	-	0.24
c1	0.19	0.20	0.21
D	8.55	8.65	8.75
E	5.80	6.00	6.20
E1	3.80	3.90	4.00
e	1.270BSC		
h	0.25	-	0.50
L	0.50	-	0.80
L1	1.05REF		
θ	0°	-	8°







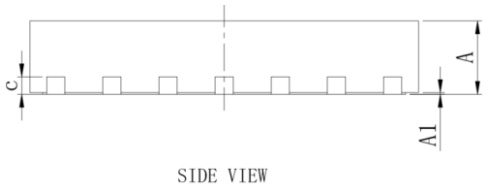


LAND PATTERN EXAMPLE (Unit: mm)

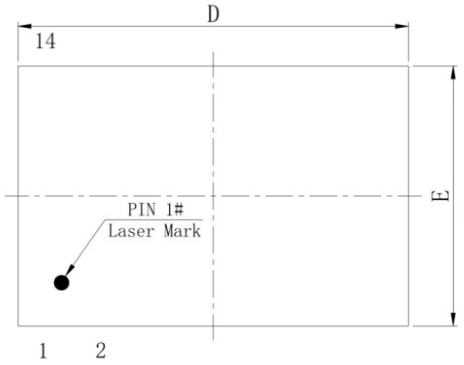
DFN4.5×3-14 DIMENSIONS

PACKAGE SIZE

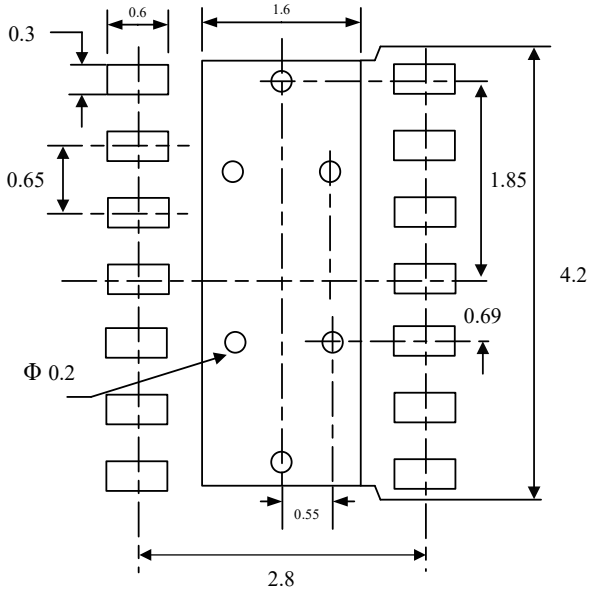
Symbol	Min./mm	Typ./mm	Max./mm
A	0.80	0.85	0.90
A1	0.00	0.02	0.05
b	0.25	0.30	0.35
b1		0.21REF	
c		0.203REF	
D	4.40	4.50	4.60
D2	4.10	4.20	4.30
e		0.65BSC	
Nd		3.90BSC	
E	2.90	3.00	3.10
E2	1.50	1.60	1.70
L	0.35	0.40	0.45
h	0.20	0.25	0.30
e		0.30REF	

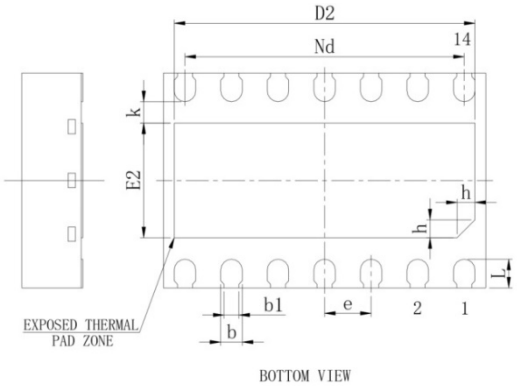


SIDE VIEW



TOP VIEW

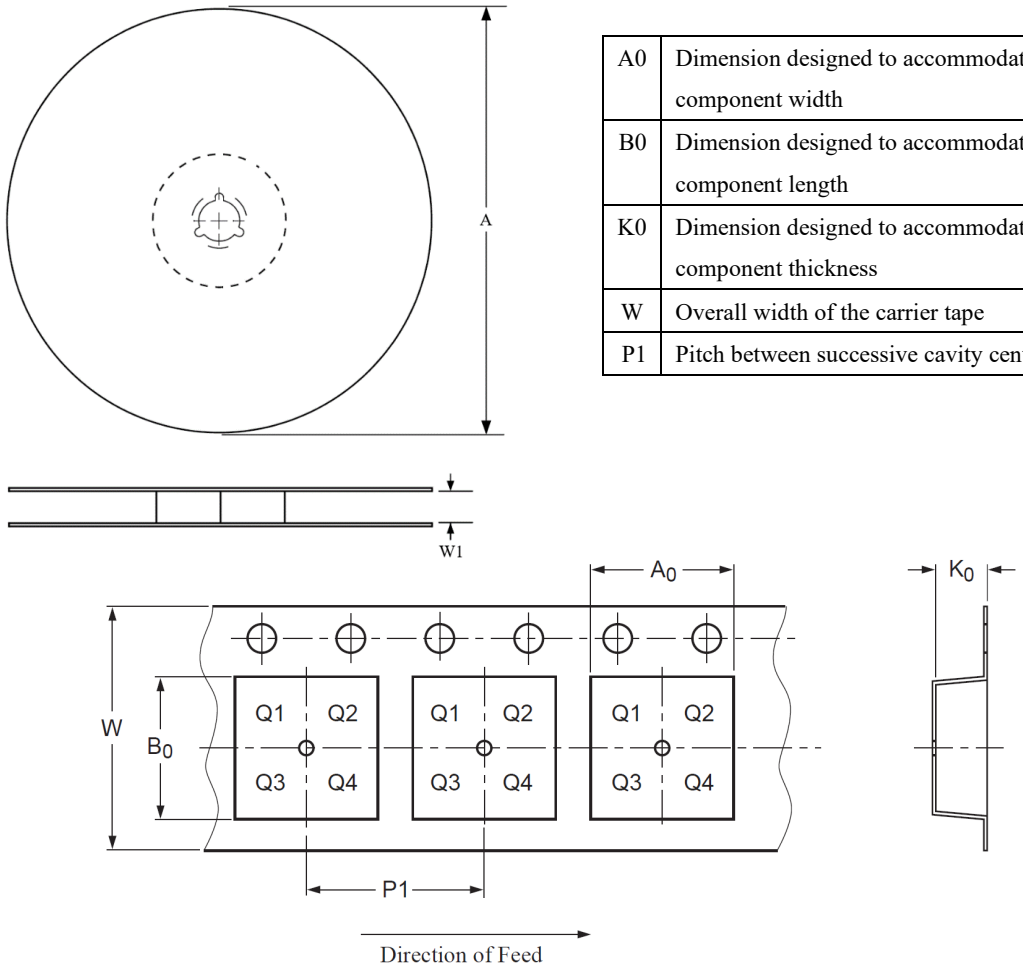




BOTTOM VIEW

LAND PATTERN EXAMPLE (Unit: mm)

TAPE AND REEL INFORMATION



PIN1 is in quadrant 1

A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

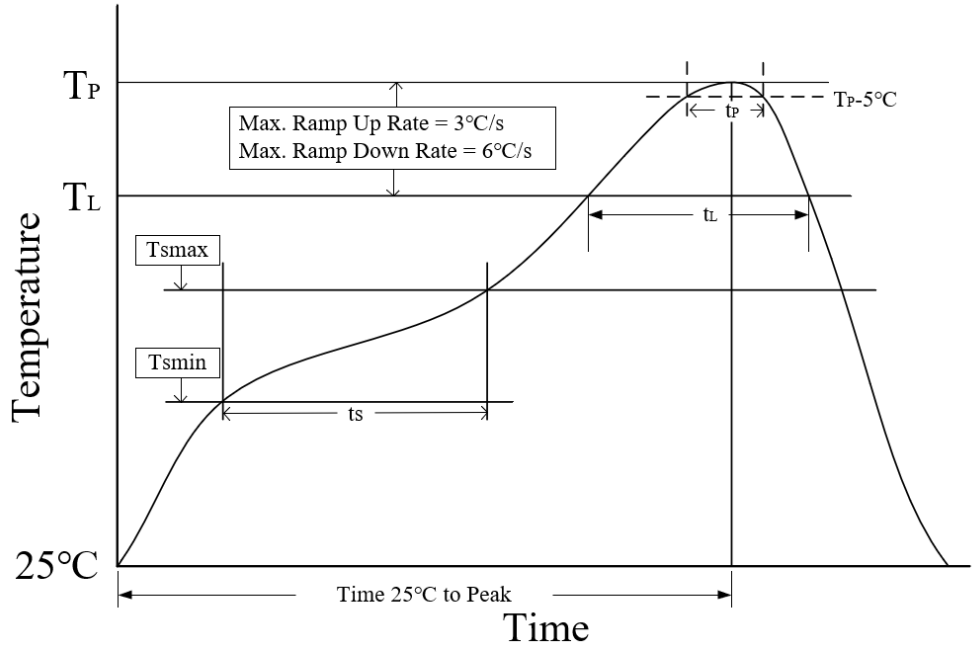
Package type	Reel diameter A (mm)	Tape width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)
SOP14	329±1	16.8±1	$6.50^{+0.20}_{-0.1}$	$9.30^{+0.20}_{-0.1}$	2.0±0.10	8.00±0.1	16.00±0.10
DFN4.5×3-14	329±1	$12.4^{+2.0}_{-0.0}$	3.75±0.1	4.25±0.1	1.00±0.1	8.00±0.1	12.00±0.3

ORDERING INFORMATION

TYPE NUMBER	PACKAGE	PACKING
SIT1022QT	SOP14	Tape and reel
SIT1022QTK	DFN4.5×3-14 small outline package, no leads	Tape and reel

SOP14 is packed with 2500 pieces/disc in braided packaging. Leadless DFN4.5×3-14 is packed with 3000 pieces/disc in braided packaging.

REFLOW SOLDERING



Parameter	Lead-free soldering conditions
Ave ramp up rate (T_L to T_P)	3 °C/second max
Preheat time ts (T_{smin}=150 °C to T_{smax}=200 °C)	60-120 seconds
Melting time t_L (T_L=217 °C)	60-150 seconds
Peak temp T_P	260-265 °C
5°C below peak temperature t_P	30 seconds
Ave cooling rate (T_P to T_L)	6 °C/second max
Normal temperature 25℃ to peak temperature T_P time	8 minutes max

Important statement

SIT reserves the right to change the above-mentioned information without prior notice.

REVISION HISTORY

Version number	Data sheet status	Revision date
V1.0	Initial version.	November 2022
V1.1	Added “LAND PATTERN EXAMPLE”; Updated “tape and reel information”; Updated “ordering information”.	January 2023