

## YGMOS Technology Crop.

100V N Channel Enhancement Mode MOSFET 100 V N 沟道增强型 MOS 管

**VDS= 100V**

**RDS(ON), Vgs@10V, Ids@1.0A = 270mΩ**

**RDS(ON), Vgs@4.5V, Ids@0.5A = 340mΩ**

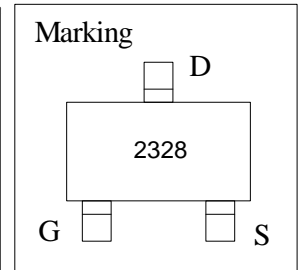
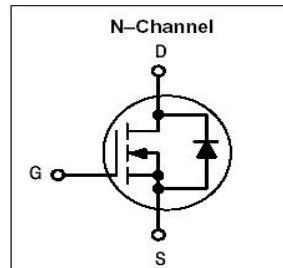
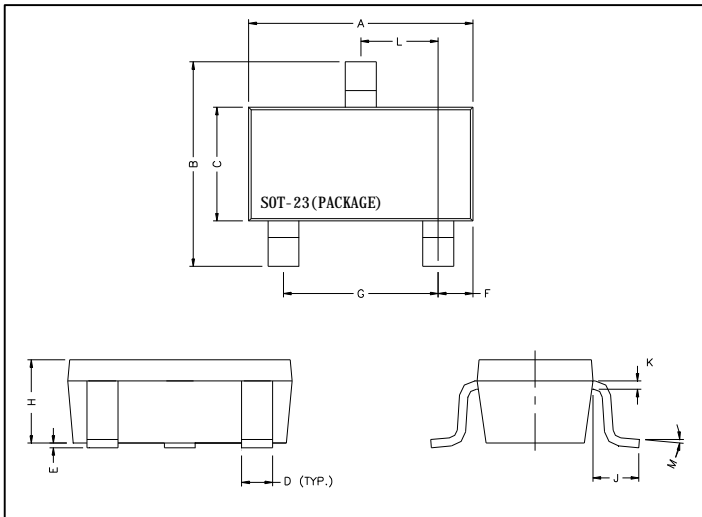
### Features 特性

Advanced trench process technology 高级的加工技术  
 High Density Cell Design For Ultra Low OnResistance  
 极低的导通电阻高密度的单元设计

Improved ShootThrough FOM 改进的成型工艺

Package Dimensions 封装尺寸及外形图

Package Dimensions 封装尺寸及外形图



REF.	Millimeter		REF.	Millimeter	
	Min.	Max.		Min.	Max.
A	2.70	3.10	G	1.90	REF.
B	2.40	2.80	H	1.00	1.30
C	1.40	1.60	K	0.10	0.20
D	0.35	0.50	J	0.40	-
E	0	0.10	L	0.85	1.15
F	0.45	0.55	M	0°	10°

### Maximum Ratings and Thermal Characteristics (TA = 25°C unless otherwise noted) 25°C 极限参数和热特性

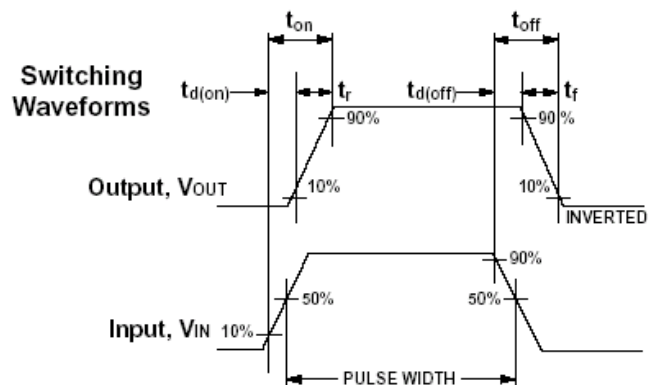
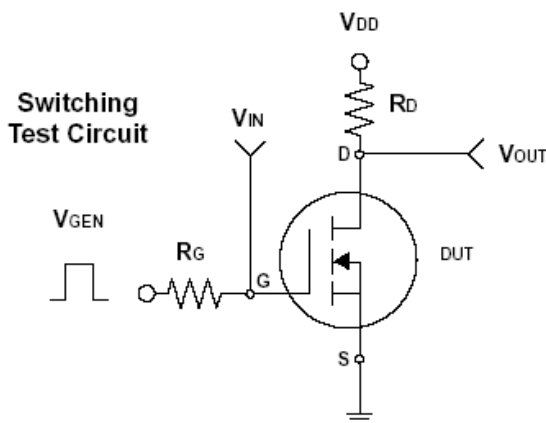
Parameter 极限参数	Symbol 符号	Limit 范围	Unit 单位	
DrainSource Voltage 漏源电压	V <sub>DS</sub>	100	V	
GateSource Voltage 栅源电压	V <sub>GS</sub>	± 20		
Continuous Drain Current 连续漏极电流	I <sub>D</sub>	1.2	A	
Pulsed Drain Current 脉冲漏极电流	I <sub>DM</sub>	5		
Maximum Power Dissipation 最大耗散功率	P <sub>D</sub>	TA = 25°C	1	W
		TA = 75°C	0.5	
Operating Junction and Storage Temperature Range 使用及储存温度	T <sub>J</sub> , T <sub>stg</sub>	-55 to 150	°C	
JunctiontoAmbient Thermal Resistance (PCB mounted) 结环热阻	R <sub>θJA</sub>	125	°C/W	

**YGMOS Technology Crop.**
**ELECTRICAL CHARACTERISTICS** 一般电气特性

Parameter 参数	符号	Test Condition 测试条件	最小值	典型值	最大值	单位
<b>Static 静态参数</b>						
DrainSource Breakdown Voltage 漏源击穿电压	$BV_{DSS}$	$V_{GS} = 0V, I_D = 250\mu A$	100			V
DrainSource OnState Resistance 漏源导通电阻	$R_{DS(on)}$	$V_{GS} = 4.5V, I_D = 0.5A$		275	340	mΩ
DrainSource OnState Resistance 漏源导通电阻	$R_{DS(on)}$	$V_{GS} = 10V, I_D = 1.0A$		230	270	
Gate Threshold Voltage 开启电压	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\mu A$	1.5	2.5	3.5	V
Zero Gate Voltage Drain Current 零栅压漏极电流	$I_{DSS}$	$V_{DS} = 80V, V_{GS} = 0V$			1	μA
Gate Body Leakage 漏极短路时截止栅电流	$I_{GSS}$	$V_{GS} = \pm 20V, V_{DS} = 0V$			±100	nA
Forward Transconductance 正向跨导	$g_{fs}$	$V_{DS} = 5V, I_D = 1A$		2.4		S
<b>Dynamic 动态参数</b>						
Total Gate Charge 栅极总电荷	$Q_g$	$V_{DS} = 80V, I_D = 1.0A$ $V_{GS} = 10V$		9.7		nC
GateSource Charge 栅源极电荷	$Q_{gs}$			1.6		
GateDrain Charge 栅漏极电荷	$Q_{gd}$			1.7		
TurnOn Delay Time 导通延迟时间	$t_{d(on)}$	$V_{DD} = 50V, R_L = 6.8\Omega$ $I_D = 1.0A, V_{GEN} = 10V$ $R_G = 3.3\Omega$		1.6		ns
TurnOn Rise Time 导通上升时间	$t_r$			19		
TurnOff Delay Time 关断延迟时间	$t_{d(off)}$			13.6		
TurnOff Fall Time 关断下降时间	$t_f$			19		
Input Capacitance 输入电容	$C_{iss}$	$V_{DS} = 15V, V_{GS} = 0V$ $f = 1.0MHz$		508		pF
Output Capacitance 输出电容	$C_{oss}$			29		
Reverse Transfer Capacitance 反向传输电容	$C_{rss}$			16.4		
<b>SourceDrain Diode 源漏二极管参数</b>						
Max. Diode Forward Current 最大正向电流	$I_S$				1.2	A
Diode Forward Voltage 正向电压	$V_{SD}$	$I_S = 2.0A, V_{GS} = 0V$			1.2	V

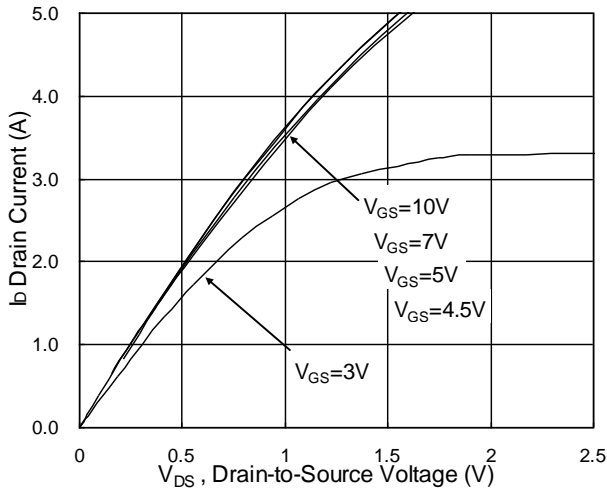
Note :

- 1.The data tested by surface mounted on a 1 inch<sup>2</sup> FR-4 board with 20Z copper.
- 2.The data tested by pulsed , pulse width  $\leq 300\mu s$  , duty cycle  $\leq 2\%$
- 3.The power dissipation is limited by 150°C junction temperature
- 4.The data is theoretically the same as  $I_D$  and  $I_{DM}$  , in real applications , should be limited by total power dissipation.

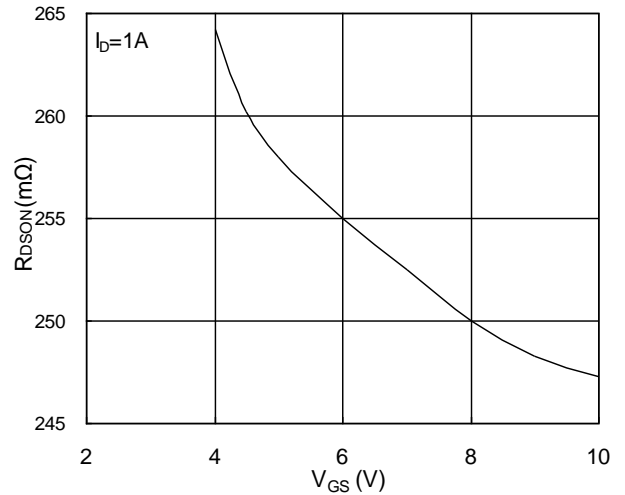


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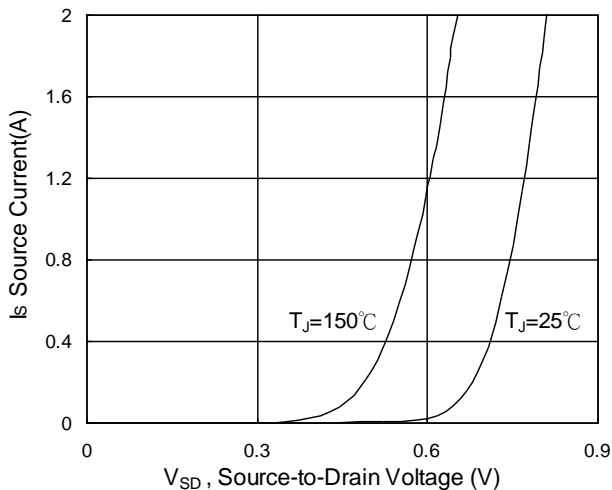
### Typical Characteristics



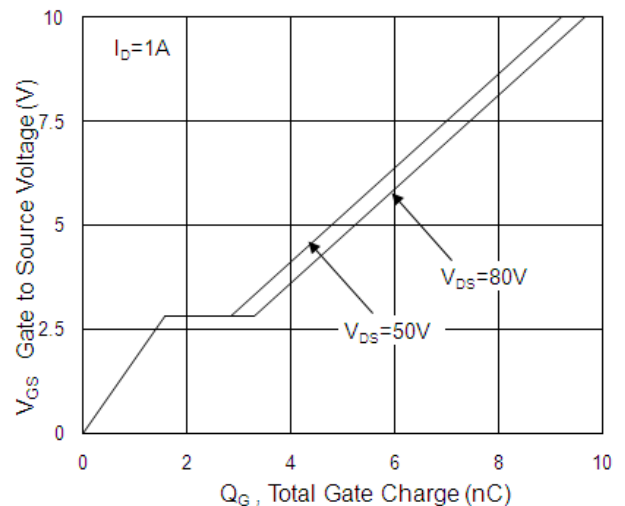
**Fig.1 Typical Output Characteristics**



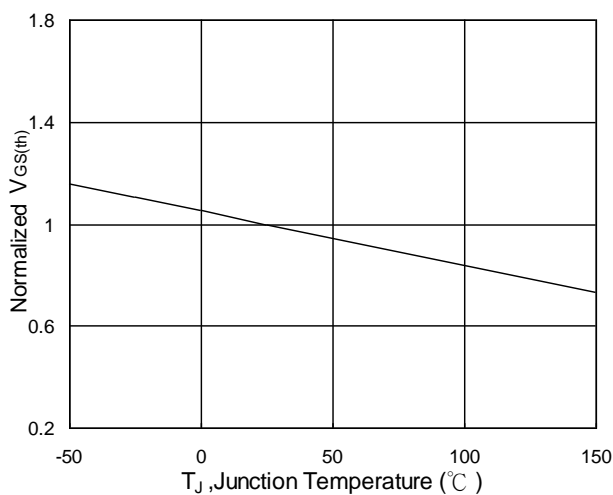
**Fig.2 On-Resistance vs. Gate-Source**



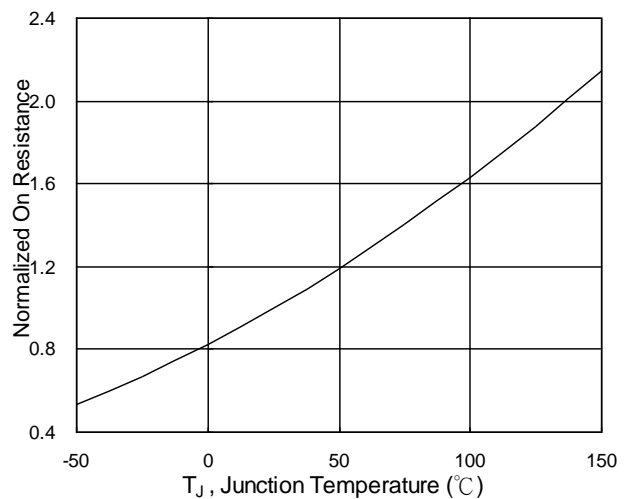
**Fig.3 Forward Characteristics of Reverse**



**Fig.4 Gate-Charge Characteristics**



**Fig.5 Normalized  $V_{GS(th)}$  vs.  $T_J$**



**Fig.6 Normalized  $R_{DS(on)}$  vs.  $T_J$**