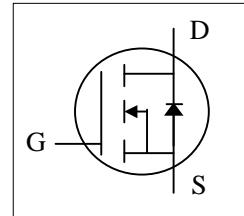




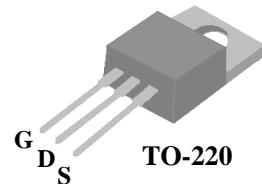
YGMOS Technology Co.,Ltd GT80N75

N-CHANNEL ENHANCEMENT MODE POWER MOSFET

- ▼ Low Gate Charge
- ▼ Simple Drive Requirement
- ▼ Fast Switching Characteristic
- ▼ Halogen Free & RoHS Compliant Product



BV_{DSS}	75V
$R_{DS(ON)}$	10mΩ
I_D	80A



Description

GT80N75 series are from YGMOS Power innovative design and silicon process technology to achieve the lowest possible on-resistance and fast switching performance. It provides the designer with an extreme efficient device for use in a wide range of power applications.

The TO-220 package is widely preferred for all commercial-industrial through hole applications. The low thermal resistance and low package cost contribute to the worldwide popular package.

Absolute Maximum Ratings@ $T_j=25^\circ\text{C}$ (unless otherwise specified)

Symbol	Parameter	Rating	Units
V_{DS}	Drain-Source Voltage	75	V
V_{GS}	Gate-Source Voltage	± 20	V
$I_D @ T_C = 25^\circ\text{C}$	Drain Current, $V_{GS} @ 10\text{V}^4$	80	A
$I_D @ T_C = 100^\circ\text{C}$	Drain Current, $V_{GS} @ 10\text{V}$	70	A
I_{DM}	Pulsed Drain Current ¹	320	A
$P_D @ T_C = 25^\circ\text{C}$	Total Power Dissipation	2	W
E_{AS}	Single Pulse Avalanche Energy ³	450	mJ
T_{STG}	Storage Temperature Range	-55 to 175	°C
T_J	Operating Junction Temperature Range	-55 to 175	°C

Thermal Data

Symbol	Parameter	Value	Units
R_{thj-c}	Maximum Thermal Resistance, Junction-case	0.5	°C/W
R_{thj-a}	Maximum Thermal Resistance, Junction-ambient	65	°C/W

Electrical Characteristics@ $T_j=25^\circ\text{C}$ (unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
BV_{DSS}	Drain-Source Breakdown Voltage	$V_{\text{GS}}=0\text{V}$, $I_D=250\mu\text{A}$	75	-	-	V
$R_{\text{DS(ON)}}$	Static Drain-Source On-Resistance ²	$V_{\text{GS}}=10\text{V}$, $I_D=30\text{A}$	-	11	18	$\text{m}\Omega$
$V_{\text{GS(th)}}$	Gate Threshold Voltage	$V_{\text{DS}}=V_{\text{GS}}$, $I_D=250\mu\text{A}$	2	2.6	4	V
g_{fs}	Forward Transconductance	$V_{\text{DS}}=15\text{V}$, $I_D=30\text{A}$	-	78	-	S
I_{DSS}	Drain-Source Leakage Current	$V_{\text{DS}}=75\text{V}$, $V_{\text{GS}}=0\text{V}$	-	-	10	μA
	Drain-Source Leakage Current ($T_j=125^\circ\text{C}$)	$V_{\text{DS}}=60\text{V}$, $V_{\text{GS}}=0\text{V}$	-	-	250	μA
I_{GSS}	Gate-Source Leakage	$V_{\text{GS}}=\pm 20\text{V}$, $V_{\text{DS}}=0\text{V}$	-	-	± 100	nA
Q_g	Total Gate Charge	$I_D=30\text{A}$	-	100	160	nC
Q_{gs}	Gate-Source Charge	$V_{\text{DS}}=60\text{V}$	-	13	-	nC
Q_{gd}	Gate-Drain ("Miller") Charge	$V_{\text{GS}}=10\text{V}$	-	47	-	nC
$t_{\text{d(on)}}$	Turn-on Delay Time	$V_{\text{DD}}=40\text{V}$	-	15	-	ns
t_r	Rise Time	$I_D=30\text{A}$	-	80	-	ns
$t_{\text{d(off)}}$	Turn-off Delay Time	$R_G=3.3\Omega$	-	67	-	ns
t_f	Fall Time	$V_{\text{GS}}=10\text{V}$	-	86	-	ns
C_{iss}	Input Capacitance	$V_{\text{GS}}=0\text{V}$	-	3703	-	pF
C_{oss}	Output Capacitance	$V_{\text{DS}}=30\text{V}$	-	281	-	pF
C_{rss}	Reverse Transfer Capacitance	f=200KHz	-	155	-	pF
R_g	Gate Resistance	f=1.0MHz	-	3.5	7	Ω

Source-Drain Diode

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
V_{SD}	Forward On Voltage ²	$T_j=25^\circ\text{C}$, $I_S=40\text{A}$, $V_{\text{GS}}=0\text{V}$	-	-	1.5	V
t_{rr}	Reverse Recovery Time	$I_S=40\text{A}$, $V_{\text{GS}}=0\text{V}$	-	80	-	ns
Q_{rr}	Reverse Recovery Charge	$dI/dt=100\text{A}/\mu\text{s}$	-	235	-	nC

Notes:

- 1.Pulse width limited by Max. junction temperature.
- 2.Pulse test
- 3.Starting $T_j=25^\circ\text{C}$, $V_{\text{DD}}=50\text{V}$, $L=1\text{mH}$, $R_G=25\Omega$, $I_{\text{AS}}=30\text{A}$.
- 4.Package limitation current is 80A, calculated continuous current based on maximum allowable junction temperature is 108A.

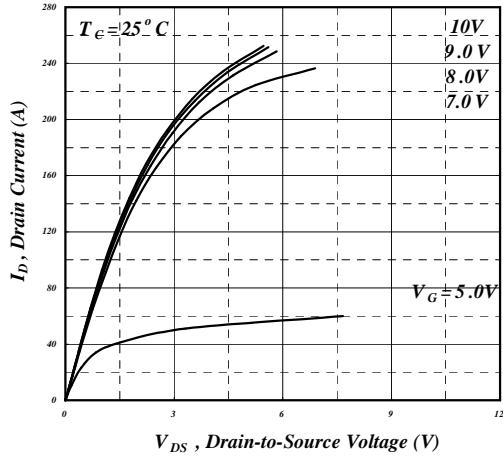


Fig 1. Typical Output Characteristics

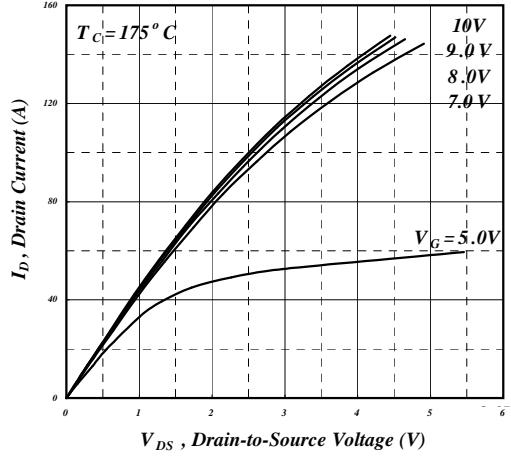


Fig 2. Typical Output Characteristics

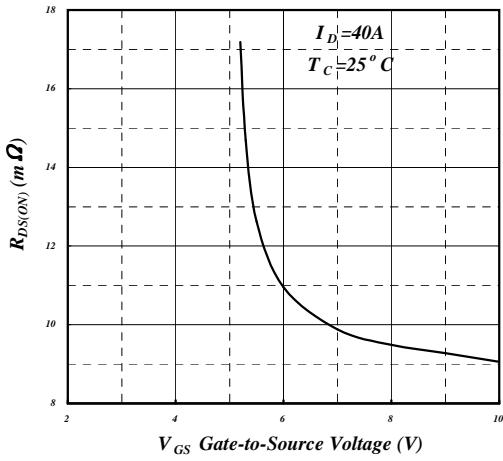


Fig 3. On-Resistance v.s. Gate Voltage

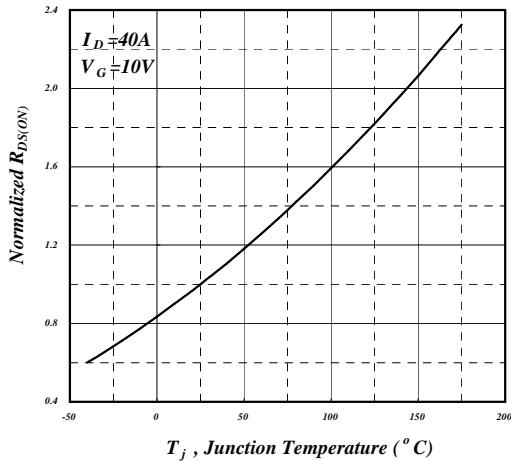


Fig 4. Normalized On-Resistance v.s. Junction Temperature

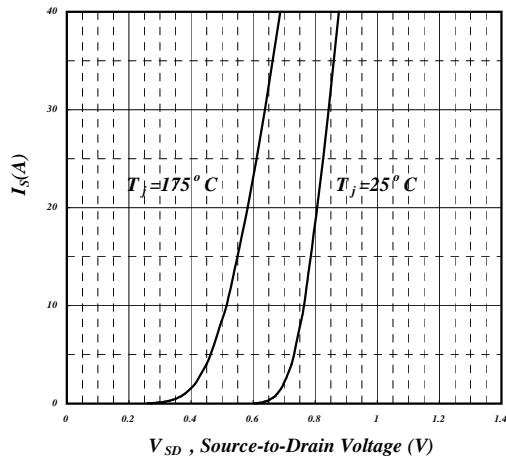


Fig 5. Forward Characteristic of Reverse Diode

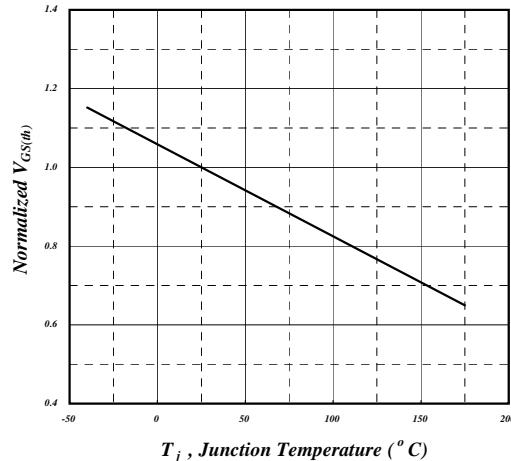
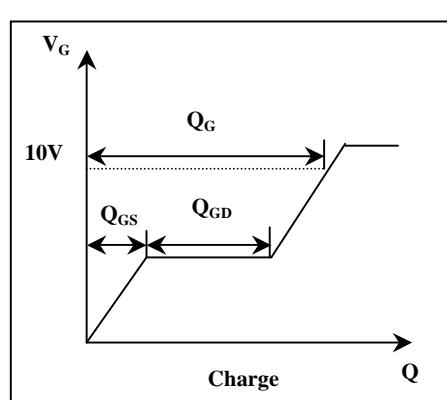
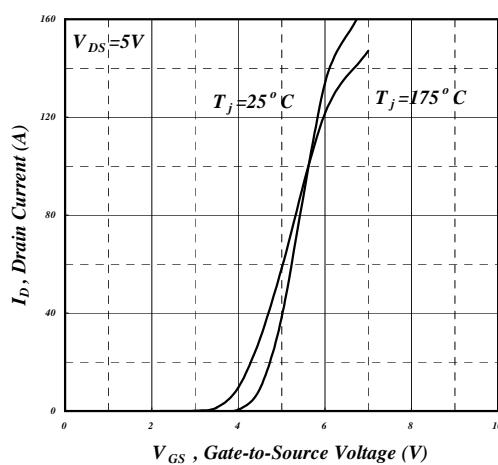
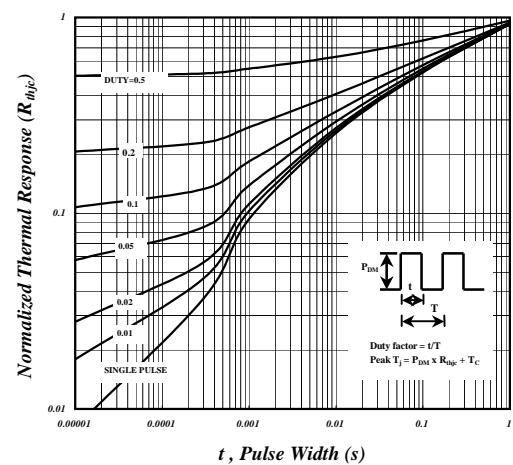
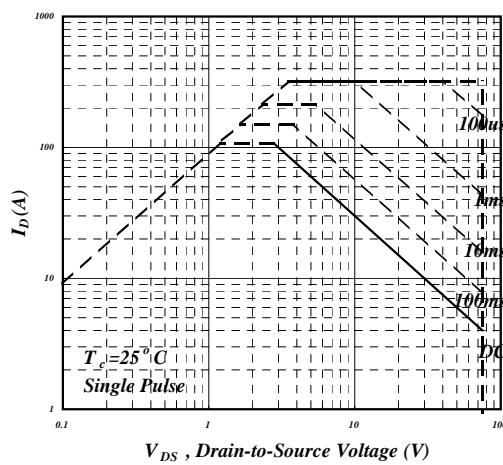
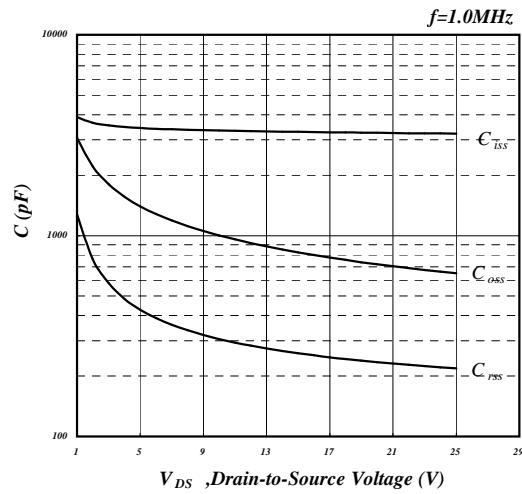
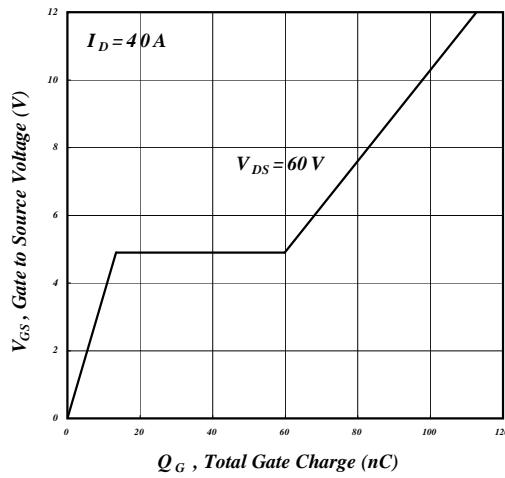


Fig 6. Gate Threshold Voltage v.s. Junction Temperature



MARKING INFORMATION

